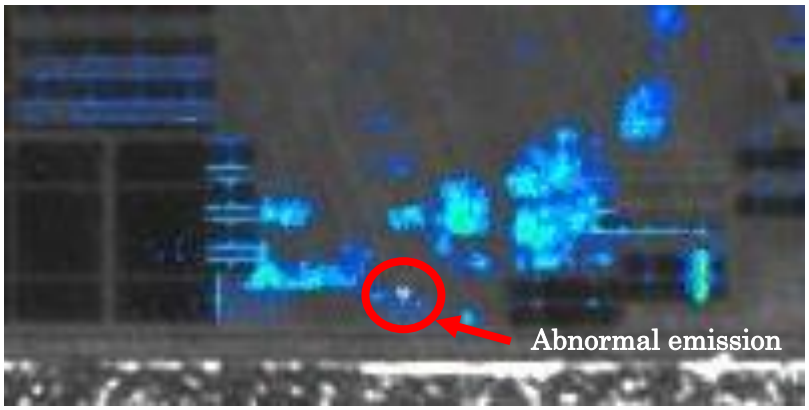
Failure Analysis Solution

Using EVA100 Measurement System



Locate product defects in a short time, and improve overall quality

- **Improve Process of Failure Analysis**
- **Increase Reproducibility with Measurement Sequence**
- **Debug Defective Part Quickly**

■ Current status and problems of failure analysis

The functions designed into Integrated Circuit (IC) have been increasing in complexity year after year. Consequently, the size of circuit has increased over the years. At the same time, continuous efforts are being made to improve the failure detection rate, and reduce the inspection time and the production costs. Even though the device failure in the field is still remaining it takes huge number of man-hours for isolating the defect in the part and to fix the failure due to design complexity.

There are still some problems, such as the defective part is a test escape during ATE production test and often the failure occurs only in the mission mode.

Therefore, more effective solutions are required.

To deal with the additional complexities:

- Increase in size of circuit (longer pattern)
- Increase in functionality（flexibility）
- Difficult to specify failure mode (failure model)
- Low reproducibility (rare)
- Failure occurring in mission mode (System Level Test)

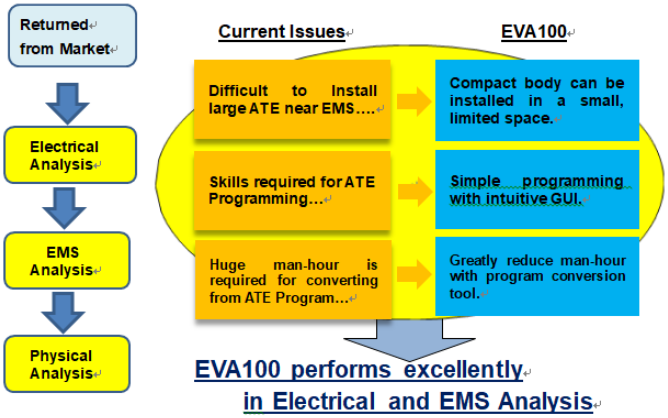


Fig.1 The effects of EVA100 in the failure analysis process

■ Failure Analysis with EVA100

Users can easily generate an inspection program for failure analysis because “EVA100” has the similarity with ATE systems used in production.

Offering the intuitive GUI environment, it is easy to operate for users who are unfamiliar to programming the complex ATE systems.

As a result, “EVA100” can seamlessly execute tests for analyzing the failure mode, while connecting with an emission microscope.

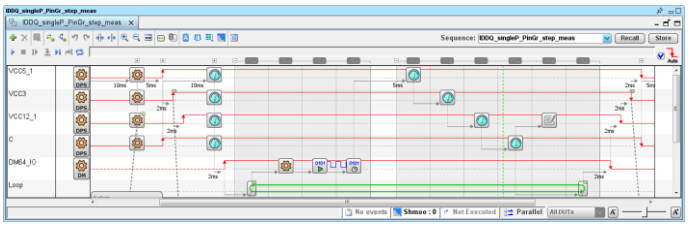


Fig.2 Measurement Sequence

■ Example of IC Failure Analysis

In the analysis methods focused on the power-supply current, the scan pattern which was used in the ATE test flow will be reused. It is easy to set up a test environment using the Pattern Conversion Software for STIL file, then specify the pattern address for monitoring the abnormal power-supply current.

After the measurement, customer can judge whether the abnormal value was caused by the individual differences or the failure by visualizing it, and isolating failing node in the IC by an emission analysis.

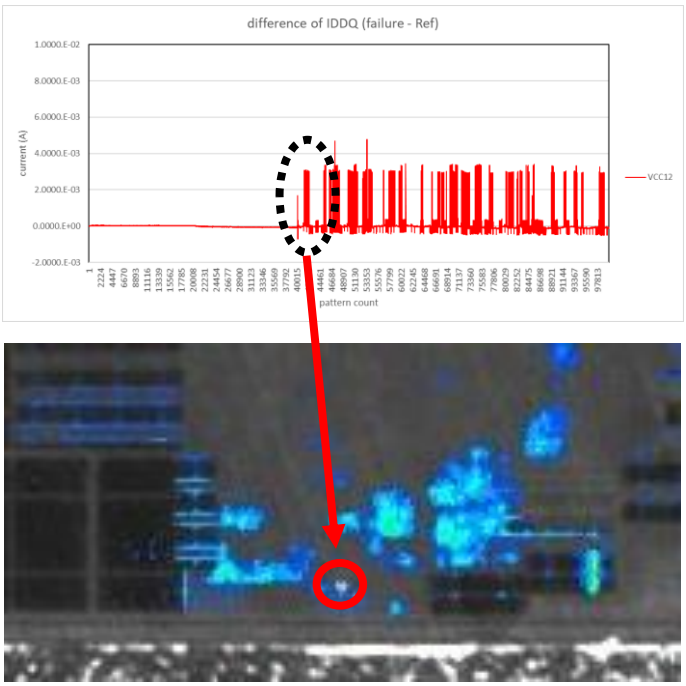


Fig.3 Graph of measured current value and Failure Analysis on IC

ADVANTEST CORPORATION
EVA Project
E-mail : info_eva@advantest.com