Advantest Corporation
IR Technical Briefing
Q&A Summary

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Q: In the future, image sensor makers will move toward 3D integration of memory circuits and logic circuits with sensors. Will this image sensor wafer stacking technology increase the number of tests required, including for peripheral circuits, and drive further expansion of the tester market as a result?

A: Stacked devices have more circuits to test, which increases test time. However, even at present, image sensors and logic circuits are tested simultaneously after the wafers are bonded together. That said, test time is mostly accounted for by the time required to test the image sensor layer. Therefore, although image sensor stacking is a positive, we currently do not anticipate that this will significantly increase demand.

Q: What kind of impact will technologies such as fingerprint recognition and face recognition have on the tester market?

A: At the moment, TDDI (the integration of touch sensor functionality into display driver ICs (DDICs)) is extending test times. This requires two touch sensor tests (ramp wave and logic) in addition to DDIC test, and the logic test alone requires 2-3x the conventional DDIC test time. Incorporating fingerprint sensor functionality will require additional analog testing, further extending test times.

Q: Your US competitor seems to be looking forward to an increase in test demand for OTA (Over the Air) and AiP (Antenna-in Packages). What business opportunities do you see for Advantest in these areas?

A: 5G RF test, including millimeter waves, requires joint technology development with customers, so we have high expectations for this business. With 5G, the number of antennas required will increase when millimeter waves are deployed. In addition, many elements of 5G RF test methods, such as parallel measurement, are yet to be established. Currently, we are working on development of this business while discussing our customers' needs with them. We agree that this will definitely be a big business opportunity in the future.

Q: The V93000 EXA Scale appears to be a strongly competitive product, and has been well received by customers. Can you confirm?

A: While refraining from direct performance comparisons with competing products, we consider that the V93000 EXA Scale outperforms all systems in its class. This redesigned platform offers advantages in speed, memory depth, throughput, and other factors that meet semiconductor testing needs in growth areas such as AI and machine learning. Those are not its only advantages. While maintaining our existing wide range of coverage from power devices to RF, which customers have always appreciated, we developed this platform for compatibility with test assets customers already own, so it inherits the customer base and the 8000 unit-plus installed base of the V93000. This, we believe, will be a strength for the future. Thus, the EXA Scale is differentiated not only by its hardware specifications, but also by these comprehensive strengths.

Q: We have the impression that automotive customers are conservative. Please share your customer development strategy in this market and your expectations for future market share growth.

A: Certainly, once an automotive customer adopts a tester, they will use it for more than 10 years, so it takes a considerable amount of time before they will consider switching testers. However, many years of customer development for both the V93000 and T2000 platforms have enabled us to successfully grow our customer base by a considerable amount. This will take some time to show up as market share, but we believe our number of customers is higher than our competitor's. Some customers are strongly oriented toward factory automation, and we also recently issued a press release announcing a joint project with one of our customers to develop test cell systems for automation. This is the key to our strategy of offering comprehensive support in terms of one-stop solutions including handlers.
From a technical point of view, high-end automotive device pin counts are increasing, and load boards (peripheral circuits that connect testers and devices) are becoming more complex, which is another challenge for automotive IC makers. Our V93000 and T2000 make it easy to design these boards, and their excellent throughput and processing speed have made automotive customers realize the benefits of adopting Advantest products.

Q: Which applications will see future growth in the SoC tester market, in your view?

A: In the short term, we sense a recovery from the Covid-19-related slump in demand for automotive, industrial, and consumer products, and our impression is that demand is increasing. In the long term, we believe that the high-end areas of 5G and HPC will see strong growth. We are also looking forward to the arrival of demand related to millimeter waves.

Q: Which do you think will be larger in the future, mobile or data center demand?

A: Against the background of the enormous smartphone market, mobile demand for devices such as application processors is significant. However, producers of HPC devices for data centers are also adopting leading-edge processes, and test times are increasing. We are discussing with our leading customers how we can make these growing test times more reasonable. The interesting thing is that there are signs of a desire for specific-purpose dedicated devices, whereas the technological trend has consistently been towards multi-purpose devices in the past. As customers take various approaches and diversify their test methods, it is important for a test platform strategy to offer products compatible with all devices, with excellent flexibility. The V93000 EXA Scale is such a platform.

Q: What are your views on future synergies between SoC testers and SLT (system level test)?

A: For complex devices, requirements are tending towards end-to-end test solutions. As the number of transistors in each semiconductor increases, the number of transistors that cannot be covered by ATE (automatic test equipment) test is becoming a problem for customers. The purpose of SLT is to improve quality and expand test coverage, but simply adding SLT will increase test costs. It is much better for the test coverage of ATE and SLT to complement and optimize each other. In these circumstances, we believe that we are the only company in a position to solve this problem, because we provide both ATE and SLT. Our SoC tester business strategy and SLT business strategy are deeply linked and have the potential to generate significant synergies.

Q: What are the results of your campaign to grow your automotive-related customer base, compared to 3-5 years ago?

A: Due to our efforts to develop new solutions, Advantest systems have been adopted by almost all major manufacturers of automotive semiconductors over the last 10 years. Currently, we are transitioning into a strategy of deeper penetration within customer portfolios, aiming to further expand our market share by providing test cell solutions.

Q: One of the testing issues raised by the evolution of SoC semiconductors is analysis capability reinforcement. With regards to this, please explain how your hardware sales business model will change in the future, and your medium- to long-term strategy, including the recently announced the partnership with PDF Solutions (PDFS).

A: Advantest started out as a measurement instrument manufacturer, and while we are still very picky about the precision of each and every electrical measurement, we also recognize that we are entering an era in which one of the big questions is how to utilize data. There is still

plenty of room for data utilization in semiconductor back-end processes, and with the increasing complexity of semiconductors, a huge amount of manufacturing data is generated every day. Thus, we are very much looking forward to our partnership with PDFS. "Advantest Cloud", built in partnership with PDFS, is a system that can collect data from the design stage to SLT, transforming the entire semiconductor manufacturing process from a series of silos into an intelligent whole, and optimizing test processes based on this analysis. In the future, we will explore synergies between measurement and data with a view to this type of optimization. Data-driven automation of test cells has become indispensable to customers, so it seems that our business will undergo major changes in the future, not only with regards to testers themselves, but also peripherals and software.

Q: There was a time in the past when the tester market shrank as a result of the adoption of design for testability, or DFT, including SCAN test. The risk of market contraction does not seem to be greater now than in the past, also because semiconductor applications are now expanding, but how do you view business risks around this point?

A: Certainly, there was a time when the adoption of DFT led to the shrinking of the market, and we are paying close attention to any possibility that this type of risk would recur. However, as explained today, we are now in the era of data, an era in which various IPs can be integrated onto semiconductors. The miniaturization of semiconductors and the adoption of advanced packaging methods have led to an increase in SCAN test patterns, and if limited to conventional test capabilities, the semiconductor industry would face difficulties. As a tester vendor, our challenge is finding the best balance between test capacity enhancement and cost increases. Under these circumstances, the risk of market contraction is becoming smaller, though it is still non-zero. Discussions with leading customers inspire confidence that the business opportunities facing us are greater than the risks.

Q: The diversification of selection methods such as Binning test is seen as beneficial for SoC test, especially for GPUs and CPUs, which are HPC applications. What is your view?

A: In the past, when the intensity ratio of the tester market was declining, testing was mainly a matter of pass / fail confirmation. But now more and more customers are seeing measurement data as valuable. Actually, pass / fail data alone is not very valuable as data. In the future, it will be key to upload manufacturing parameters and test results to the cloud to understand how they interact, and feed back to the entire process. This is also the background of our partnership with PDFS. We expect that this type of demand will increase in the HPC area in the future.

Q: How much has the performance of the V93000 improved in the last 10 years? And how much performance improvement do you expect in the next 5 to 10 years?

A: The previous generation of the platform, the V93000 Smart Scale, was released about 10 years ago and is still used as a main test platform together with module upgrades. The V93000 EXA Scale was also developed as a platform with performance that can meet customer requirements 10 years from now by taking on technical challenges in anticipation of future device trends, such as the adoption of advanced packages and parallel processing architecture. In terms of specifications, features include an increase in the number of pins (from 128 pins to 256 pins) and an increase in the maximum operating frequency (from 1.6 Gbps to 5 Gbps).

Q: How do you determine tester specifications? Are the performance improvements of the EXA Scale a result of your company's technical pace? From the outside, it looks as if the structural changes on the tester side and evolution on the device side are moving in step, roughly speaking. As a result, test times do not change much on average.

A: Generally, this is the case, but customers have called for a new platform to solve production issues associated with the adoption of advanced device processes such as 5nm / 4nm / 3nm. In mature processes, some test items have no longer been required, but when customers shift to more advanced processes, they need to test more items, which leads to an increase in test times.

Q: Customers definitely don't want to waste money on test, but more applications need to be tested in the first place, which increases test intensity. Does that mean that Advantest is responding to the test needs generated by these technological realities?

A: We think so.

Note

This document is prepared for those who were unable to attend the information meeting and is intended only for reference purposes. The original content has been revised and edited by Advantest for ease of understanding.

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