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Advantest IR Technical Briefing

# Test Needs and Solutions in the Memory Semiconductor Market

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# NOTE

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## Agenda

✓ Memory Tester Business Environment

✓ Test Needs and Solutions in the Memory Semiconductor Market

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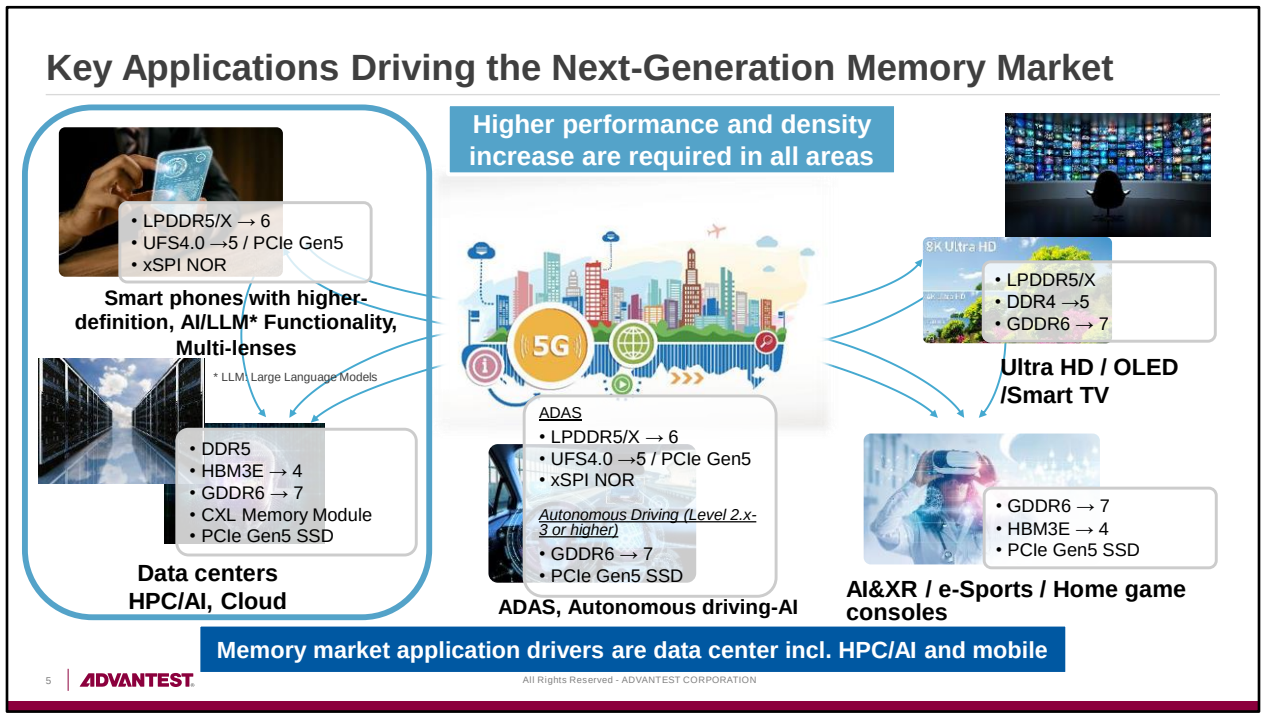
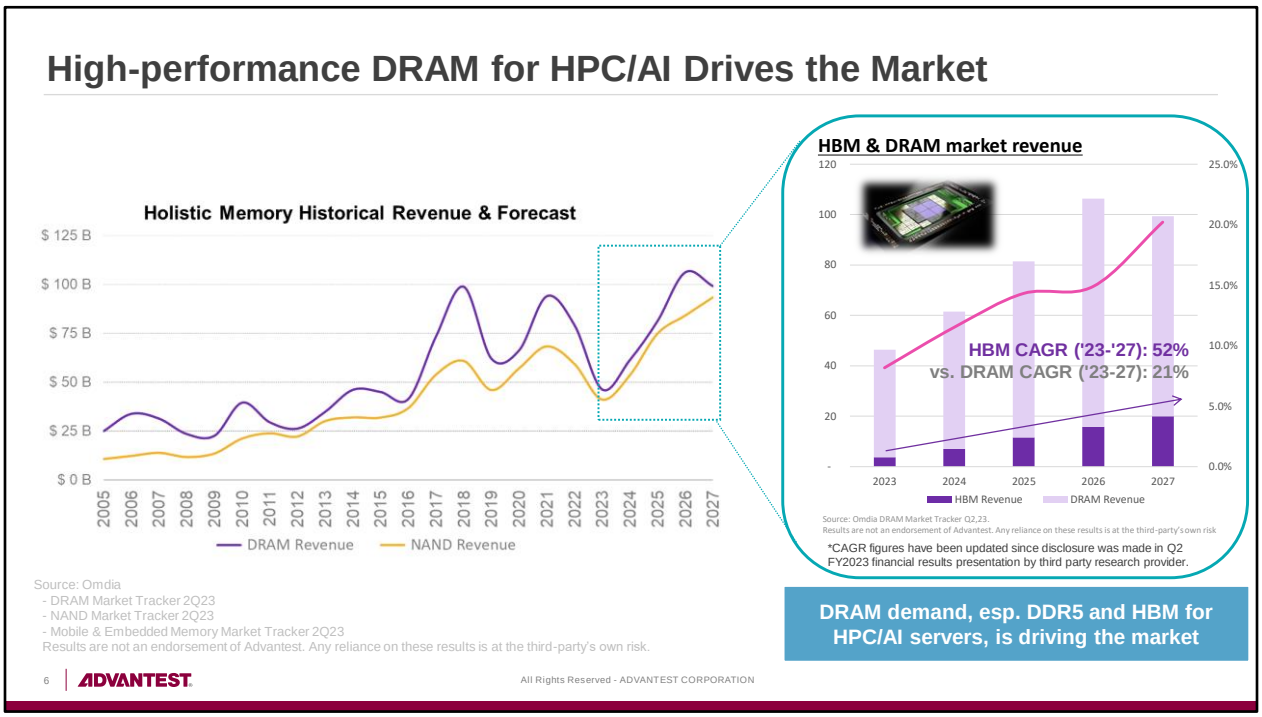
# Memory Tester Business Environment



- Hello. I am Suzuki.
- I will explain about our memory tester business environment.




- Semiconductors support "safety, security, and comfort" in our daily lives. The applications of semiconductors are expanding, and technological advancements are making our lives more convenient and comfortable.
- In memory semiconductors as well, more and more memory semiconductors are being used as the range of applications expands. In addition, memory semiconductors are undergoing an increase in density and performance, given continuous advancement of end products continues to evolve.
- This slide shows the major applications that will drive the next-generations of memory market.
- In particular, memory semiconductors used in smartphones and servers in data centers, are driving the memory market with higher functionality and increased density. These are displayed on the left hand side of the slide.
- In addition to the evolution of performance in smartphones, such as higher-definition and multi-lens cameras, recently, functions such as AI and large-scale language models (LLMs) are being deployed.
- The emergence of new technologies such as generative AI is also expected to drive further capacity expansion of data centers in the server-related sector.
- Accordingly, memory semiconductors are expected to see higher performance and increased density, as well as an expansion in supply.




- In high-performance memory, DRAM for high-performance computing (HPC) and AI are expected to be the main drivers of the memory market , along with smartphones.

- The graph on the left side of the slide shows sales of DRAM and NAND Flash in the overall memory market. Since 2017, the baseline of memory semiconductor market size has increased compared to the past, supported by expanded smartphone functionality and growing demand for data centers.

- Under those circumstances, we saw an increase in demand for 3D NAND Flash products as well as a rise in added value and supply of memory products alongside technological advancements, such as the transition to the DDR4 generation.

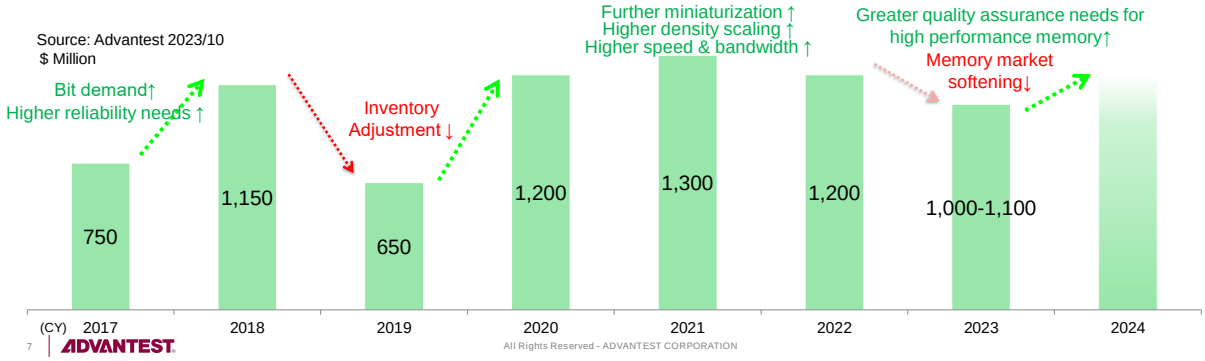
- This year, in 2023, market conditions are deteriorating due to continued inventory adjustments by memory semiconductor manufacturers and falling investments in consumer and data center applications. However, the overall memory market is expected to expand rapidly going forward due to expectations for a rapid increase in demand for high-performance memory, inspired by factors such as generative AI.

- The market forecast for HBM is for a 5 year CAGR is approximately 52% over the next five years from a period of 2023 to 2027, which is higher than the average growth rate of around21% for DRAM as a whole over the same period.

## Memory Tester Market Trends

- **Density increase, higher interface speeds**, and **higher reliability assurance** are key determinants of an increase in tester demand
- In comparison with the previous down cycle (2019 vs 2023), the decline caused by the memory market deterioration is somewhat offset by an increase in tester demand for high-performance memory such as HBM and DDR5
- In 2024, the market is expected to expand year-on-year due to a recovery in market conditions and an increasing demand trend for high-performance memory

**Memory Tester Market Transforming into a Less-Cyclical Growth Market**



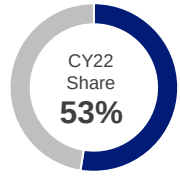




- We would now like to explain how the memory tester market has been trending in the memory semiconductor market.
- The memory tester market is affected by fluctuations in memory semiconductor production volume. However, more than production volume, factors such as increasing density, faster interfaces, and higher reliability assurance are the main drivers for growth in tester demand of memory semiconductors.
- During the previous down cycle in 2019, the memory tester market shrank by more than 40% from the previous year due to deteriorating memory semiconductor market conditions and inventory adjustments.
- Turning to 2020, the shift to DDR5 generation in LPDDR for smartphones began, leading to an increase in tester demand. An increase in memory density led to an increase in demand for tester volume, while faster interface speeds led to replacement demand for next-generation testers.
- In the most recent down cycle of 2023, the size of the tester market has also been affected by the memory market. However, compared to the previous decline, we expect the trough to be shallower, as there will be some offsets from a certain amount of increased tester demand for high-performance memory such as HBM and DDR5.
- Going forward, in addition to the recovery of the memory market, we expect the market size to expand in 2024 due to the strengthening of testing to ensure "high reliability" in high-performance memory. This is already stimulating tester demand in the near term.
- We feel that the memory tester market is transforming into a less-cyclical growth market compared to the past, although it is still subject to fluctuations in semiconductor production volume.

## Core competence to maintain the world's No.1 memory ATE* market share

- **Strong technology capabilities and leadership in the memory test industry**
  - Memory ATE market share in 2022 : 53% (Advantest estimate)
  - First to market optimal test solutions in the high-end market
    Consistently establishing a de facto standard position in the industry
- **Industry's No.1 product portfolio and total solution capabilities**
  - Extensive product portfolio for all test processes
    Competitive advantage through comprehensive solutions including peripherals
  - Enhancing customer's volume production efficiency through
    high product quality that delivers the industry's highest MTBF**
- **The industry's largest and robust customer base**
  - Globally positioned expert engineers with the advanced memory testing knowledge and experience accumulated over the years

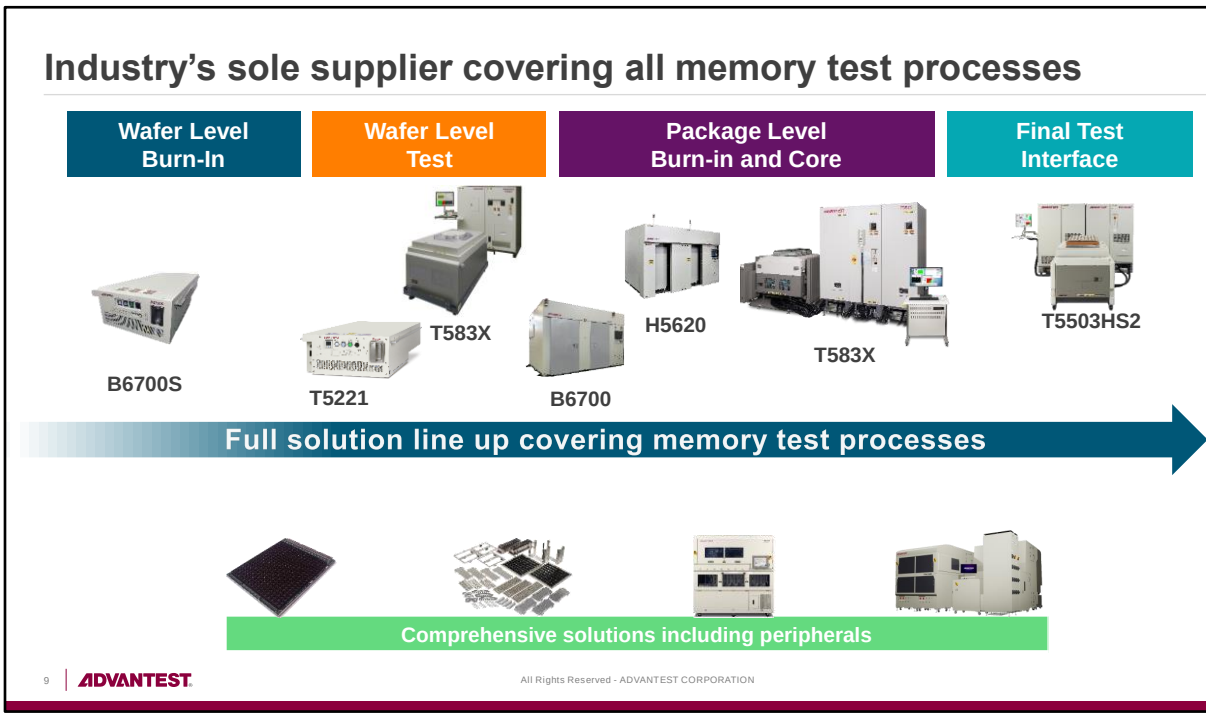



Source: Advantest


*ATE: Automated Test Equipment
**: Mean Time Between Failure




- Next, I will explain our position in the current memory tester market. We have three major core competencies.
- The first is our advanced technological capabilities and leadership in the memory test industry.
- Since the 1990s, we have continued to provide close technical support to customers developing leading-edge technologies, and for more than30 years, we have accumulated a wealth of experience and solid technical capabilities in memory testing by closely following the technological evolution of memory semiconductors.
- For the year 2022, we have maintained our leading position in memory testers with an estimated 53% market share. By being the first in the industry to launch optimal test solutions, especially for high-end memory, we have consistently established a de facto standard position in memory testers.
- Second, we have the industry's No. 1 product portfolio and comprehensive solution capabilities. In addition to a product portfolio that covers the entire memory test processes, which we will touch upon in the next slide, we are also able to offer comprehensive testing solutions, including peripheral equipment, which gives us a competitive advantage. Our industry-leading product quality with low failure rates helps our customers maximize their volume-production efficiency.
- Third, we have established the industry's largest and most solid quality customer base. Our expert engineers, who embody the advanced memory test knowledge and experience we have cultivated over the years, are positioned globally to provide timely technical support for everything from memory semiconductor development to volume production, earning us the trust of a wide range of customers.




- This slide shows one of our core competencies introduced on the previous page, a product portfolio that covers all memory test processes.

- By proposing a combination of our technology-driven product lineup, from device interfaces to test handlers, which are test-related peripherals, we are able to provide our customers with comprehensive support for setting up test environments. This is a factor which differentiates us from our competitors.

## Integrated solutions for memory device technology evolution & supply growth

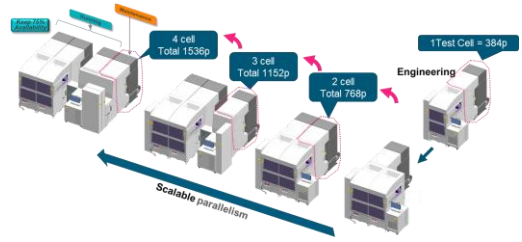
**Memory test cell "inteXcell" offers extensive test coverage with integration of high throughput handling technology**

- Industry-leading test solutions that integrate the memory test, device interface, and auto handler technologies we have accumulated over the years
- InteXcell addresses memory device package testing challenges such as higher density, power savings, and higher interface speed
- Single platform that covers design evaluation to mass production

inteXcell Series 4Cell Configuration

**Combines scalability of system configuration with minimized footprint**

- Flexibly expand parallelism from 364 to 1,536 DUTs*
  *DUT: device under test
- Footprint reduced to aprx.1/3 of that of conventional products
- Contributing further to production efficiency by controlling each small test cells individually and addressing automation at customers' volume production facilities







- Lastly, I will provide another example of how we can help customers set up a comprehensive test environment.
- The product on this slide called inteXcell, which is an industry-leading test solution that integrates memory test, device interface, and auto-handler technologies.
- This is an industry-leading integrated solution that responds to the technological evolution and an increase in supply of memory semiconductors, for which demand is expected to grow over the medium to long term.
- It is a state-of-the-art solution that addresses the challenges associated with package testing of memory devices, such as higher performance, lower power consumption, and faster interfaces.
- Operationally, the most important feature of inteXcell is its scalability in system configuration and its ability to minimize footprint. The solution contributes to higher utilization rates by supporting control of each small test cell individually in the volume production process and facility automation, while at the same time reducing footprint to about 1/3 of that of our conventional products.
- We were able to design a very compact chamber structure for setting the temperature environment during testing. Improved thermal efficiency helps reduce power consumption required to set a wide range of temperature environment ranging from high to low.
- This new solution will support our customers' technological evolution while at the same time helping to improve production efficiency and energy efficiency of testing.
- This concludes my presentation.


- Hello. I am Yokoyama.
- My presentation, titled Memory Semiconductor Testing Needs and Solutions, will focus on HBM, a type of graphic DRAM that has received the most attention in the memory industry recently

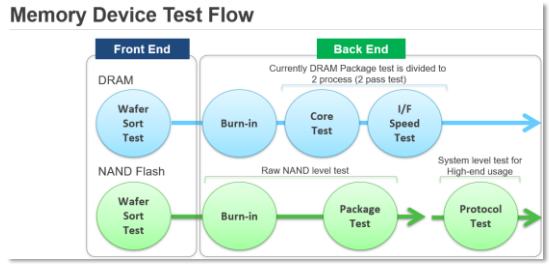
## Memory Semiconductor Test Flow and Features

### Memory Test Features

- Test flow set up from wafer to package according to test menus and temperature environment
- High parallelism is crucial to optimize throughput according to the technological evolution of memory
- Requirements becoming more rigorous as generation changes have led to higher test speeds and higher reliability assurance needs

### Key drivers of memory test/tester demand

- Bit growth (# of chip shipped x memory density) is critical to test demand
  Transition to advanced processes such as miniaturization of DRAM and increasing 3D-NAND layer count leads to bit growth and longer test time, causing tester demand to grow for each test flow
- Rise in memory data transmission speed creates new demand for high-speed testers
  DRAM interface speed test process requires testers with new test coverage
- Increase in production volume of high-performance memory semiconductors for AI/HPC with high reliability requirements
  For HBM, tester demand increases due to more elaborate testing and additional test insertions post stacking driven by higher reliability requirements alongside adoption of advanced packaging








- First, I will provide an overview of memory semiconductor test flows and explain memory test characteristics as well as the main drivers of tester demand.

- Please see the upper right corner of this slide. This slide shows a simplified test flow for a typical DRAM and NAND device. Both DRAM and NAND go through a burn-in test process under high temperature to eliminate initial defects, and then a test process to verify that semiconductor functions as designed through highly precise electronic signal analysis. There are many test processes. Conditions such as temperature settings are added to the test process, and devices undergo tests many times.

- As shown in the lower right-hand corner of this slide, there are test needs and technical challenges for each process in memory semiconductor testing. In general, testing conditions become more demanding, as the semiconductor goes through a number of steps, from the wafer test to the final package test.

- In DRAM, for example, memory interface (I/F) speeds continue to increase with generational changes, such as DDR4 to DDR5. Accordingly, post-packaging testing is divided into burn-in and core test at actual operating speeds, and I/F speed test to test DRAM at high-speed.

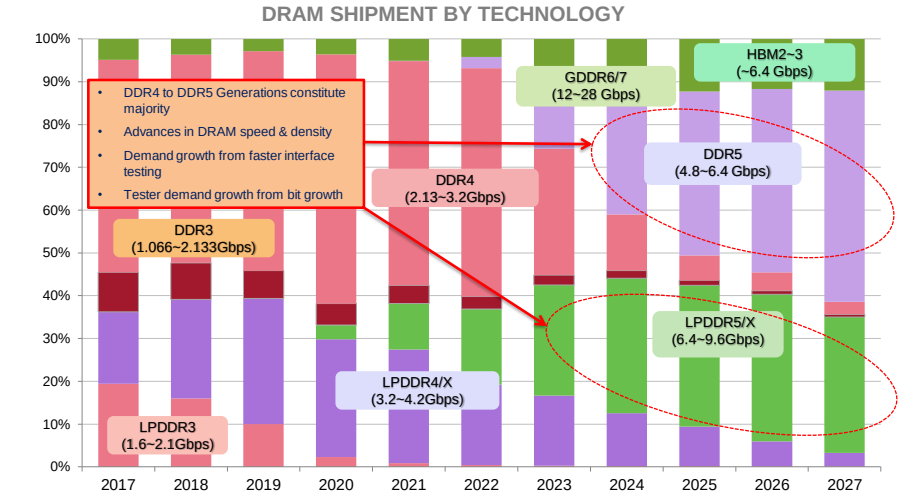
- Demand for memory semiconductor testers arises primarily from three factors.

- The first is bit growth, which is a multiplication of the number of chips shipped and density. Bit growth results in longer test time and drives tester demand throughout the test flow.

- The second is the increase in memory data transmission speed. This causes demand creation for high-speed testers with new test coverage.

- The third is the increase in production volume of high-performance memory semiconductors for AI/HPC and other applications, and the requirement for high reliability. We will explain these in detail in the following pages.

## DRAM Interface Trend Forecast




Source: Omdia DRAM Market Tracker Q2.23.
Results are not an endorsement of Advantest. Any reliance on these results is at the third-party's own risk



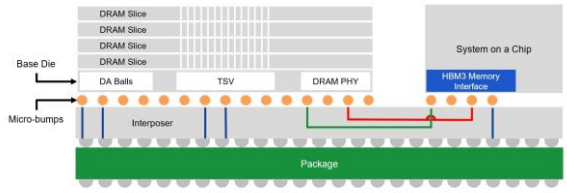

- This slide shows technology trends and future prospects for DRAM interfaces, including high-performance memory, which is expected to drive the memory semiconductor market.
- In this chart, the composition of each DRAM device is in terms of bit conversion. Bars from 2017 to 2022 are based on actual results, bars from 2023 to 2027 are based on forecasts.
- From 2023 to 2024, the generation shift to DDR5, mainly for PCs and servers, will continue, and DRAM speeds and density will continue to increase. In addition, LPDDR, a low-power consumption device mainly used in mobile and automotive applications, is also expected to see higher speeds and density, and demand for LPDDR5/X is also increasing in data centers. The transition to the DDR5 generation will create demand for higher interface speed testing and will also lead to increased demand for tester volume due to bit growth.
- HBM, which is at the top of this chart, also continues to increase in speed and density. Against a backdrop of higher quality requirements from end products, elaborate testing is being carried out to increase the percentage of good devices, and there has been a steep rise in tester demand as we speak, including longer test time and additional test insertions. Although the percentage of HBM in the total DRAM market is expected to be around 10%, we expect to see a rise in demand for testers driven by “density increase,” “higher interface speeds,” and “higher reliability assurance."

## High-bandwidth memory HBM supporting social implementation of gen. AI


**Rapid spread of gen. AI such as ChatGPT & advanced LLMs**
**Sharp demand acceleration of for high-performance AI modules (GPU+HBM)**
**(HBM market: 52% CAGR projected over 2023-2027)**

### What is HBM (High Bandwidth Memory)?

- A type of 3D stacked memory technology. Higher bandwidth and density scalability than conventional 2D memory
- Challenges exist for advanced packaging such as 2.5D/3D with increased manufacturing costs and thermal control.
  Used primarily in high-performance HPC/AI computing
- Latest HBM3 offers 12 times higher density and 13 times higher bandwidth than GDDR6




HBM3 Memory Interface (Source: Rambus Inc.)

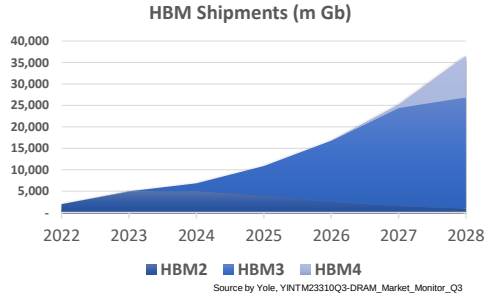
**High market growth rate is expected as GPUs with high parallel processing with thousands of cores or more and HBM with its optimal configurations are essential for AI technology, which requires enormous computing power**




- Let me briefly explain about HBM, which is now expected to grow at the highest rate.
- Since the end of last year, the rapid market expansion of generative AI and advanced LLM has accelerated the demand for high-performance AI modules in semiconductors such as GPUs and HBMs.
- As shown on the right side of the slide, HBM uses 3D stacked memory technology to provide higher bandwidth and density scalability, and side-by-side connection on the same substrate with the latest SoC semiconductors, such as GPU and custom ASIC, provides higher processing power, thereby supporting higher performance of the entire system.
- Although today's HBM is said to face challenges for the next stage of further scaling due to manufacturing costs and thermal control issues, further performance improvements are being deliberated as the learning curve picks up for next-generation stacking technology.
- These GPUs with high parallel processing capability with thousands of cores or more and HBM with its optimal configuration are essential for future AI technology, and therefore the market is expected to grow at a high rate.

## HBM Technology Trends and Outlook

**Rapid expansion from HBM3 to HBM4 generation over the next 5 years, led by AI modules for data centers**




Source by Yole, YINTM23310Q3-DRAM_Market_Monitor_Q3

- HBM CAGR of 49% from 2023-2028 (bit base)
- Rapid share expansion of HBM3 (incl. enhanced versions) after 2024
- New process development, addressing issues such as thermal and cost, is expected for the next generation HBM

**Interface speed, bandwidth, stack count, and density expected to double with each generation**

Performance Comparison by HBM Generation

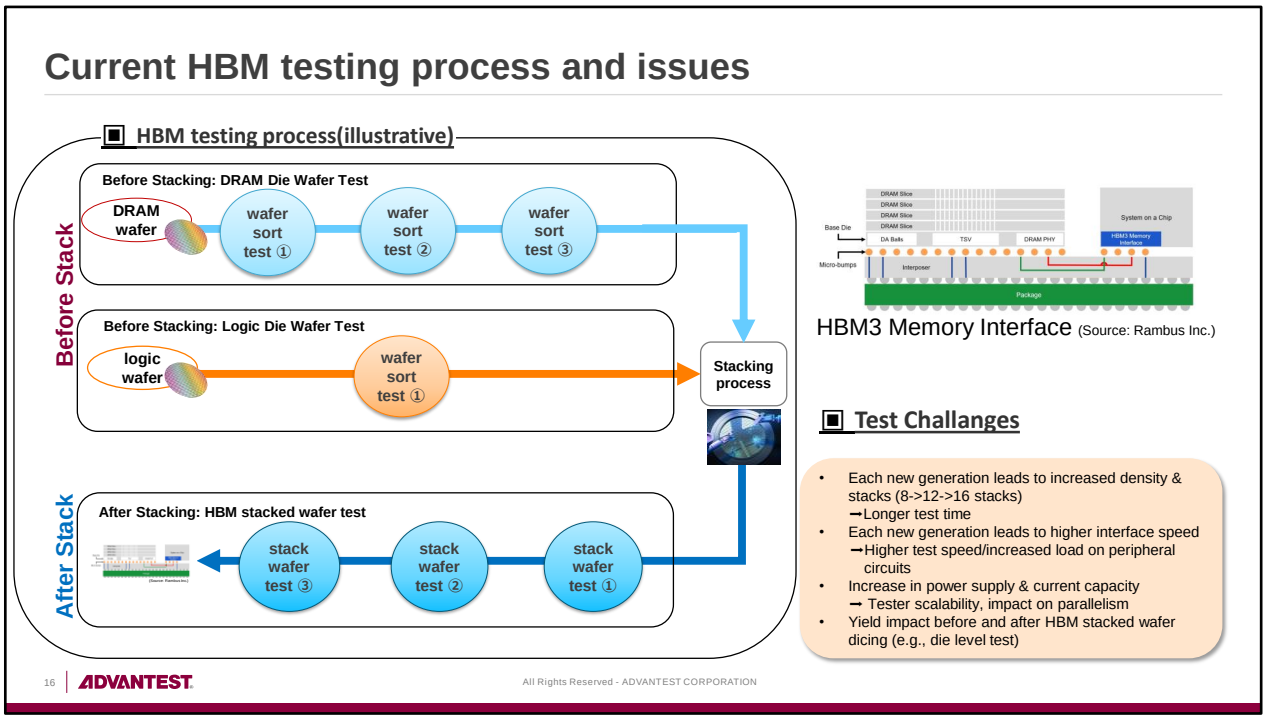
| | HBM2E | HBM3 | HBM4 |
|---|---|---|---|
| **Memory bandwidth** | 460GB/s | >820GB/s | >1.5TB/s |
| **Density per die** | 8/16Gb | 16/24Gb | 24/32Gb |
| **Stack count** | 4, 8 | 8, 12 | 8, 12, 16 |
| **IO Speed** | 3.2 Gbps | >6.4Gbps | TBD |

Includes Advantest Marketing Estimation

- Bandwidth performance growing multiple-fold from HBM2E, HBM3, its enhanced versions, and to HBM4 generation
- Memory density increases as the HBM stack count changes to 4-8-12-16 stacks, along with the miniaturization of the individual die

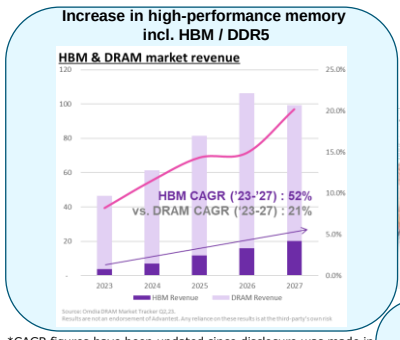



- We will now explain HBM technology trends and future prospects.
- The graph on the left of this slide shows shipment of HBM on a bit basis. Over a five-year period from 2023 to 2028, growth rate of about 50% is expected.
- The table on the right side of the slide is a comparison of HBM performance improvements expected from generation transition. Our marketing department compiled trajectories from HBM2E to HBM4, based on the evolution by memory bandwidth, density per die, stack count, and speed.
- The current mainstay HBM2, 2E, has density of 8Gb or 16Gb per die and has 4 or 8 stacks. Speed is estimated to be 3.2Gbps or higher are.
- As we move into the next generation of HBM3, its enhanced versions, and HBM4, we expect to see a 1.5x to nearly 2x increase in density per die and stack count, as well as a nearly doubling of speed and total memory bandwidth.
- Such scaling and scalability is directly related to increased testing demand.

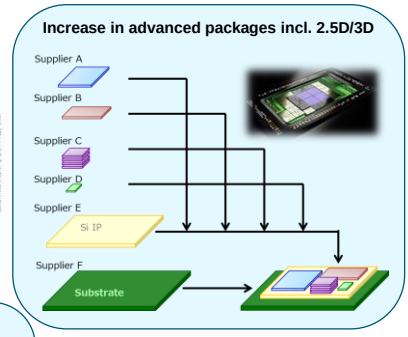


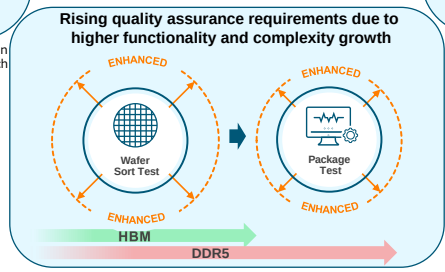

- The following is a simplified image of how memory manufacturers are currently testing HBM and the challenges they face in testing.
- The figure on the left shows an image of the testing process from the time the DRAM wafers that make up the HBM and the logic wafers that serve as the interface are manufactured to the time the HBM is shipped.
- The light blue DRAM wafers shown at the top are likely to undergo a testing process similar to that of conventional DRAM memory. The orange logic wafer in the middle will also undergo a simple wafer test. The HBM wafer is then completed via the 3D stacking process at the intersection of the light blue and orange arrows.
- The process then shifts to the post-HBM stack process in blue at the bottom. Multiple test insertion are likely to take place such as memory cell access and functional tests. Quality will be improved by undergoing those multiple test insertions, and they will be shipped finally.
- Going forward, as the HBM market expands and memory performance improves, various test challenges are expected, including memory density increase driven by an increase in stack count, rising interface speed, and impact on parallelism from an increase in device power supply as well as electric current. In order to handle such challenges, testers need to harness greater scalability.
- In addition, in response to yield impacts from dicing of HBM wafers, countermeasures such as introduction of die-level testing post dicing is being discussed.
- Currently, we have a high share of the HBM market. We will continue to research and develop the best solutions for future needs in a timely manner, by anticipating all possibilities and by taking advantage of our broad product portfolio.

## Business opportunities for memory testers arising from gen. AI




*CAGR figures have been updated since disclosure was made in Q2 FY2023 financial results presentation by third party research provider.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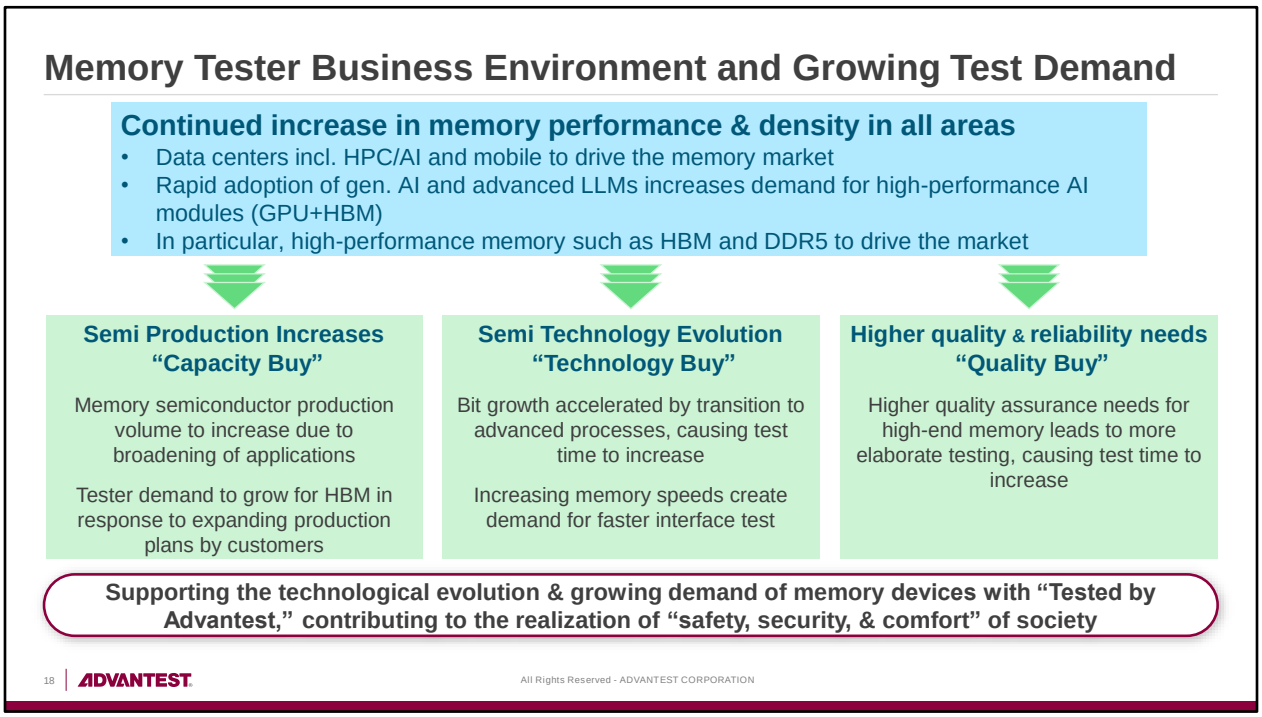
- Social implementation of generative AI has just begun.
- Driven by demand related to generative AI, high-performance memory, such as HBM and DDR5, are expected to enjoy high market growth.
- As packaging capacity for advanced packages such as 2.5D and 3D increases, production volume of such high-performance memory is expected to grow.
- In addition, test parameters and test processes are being enhanced in terms of further quality assurance of semiconductors as they become more performant and gain complexity.
- As a result, we see further opportunities for our memory tester business, which we believe will be the key to future growth.




- Finally, we will summarize the business environment for memory testers and the expansion of test demand.

- As explained at the beginning, memory semiconductors are continuing to increase in performance and density in all domains. Among these, in particular, we expect the technological evolution and market growth of HBM and DDR5, which are high-performance memories, to drive the market going forward.

- We will continue to lead the industry and contribute to the realization of "safety, security, and comfort" in society by firmly supporting the technological evolution and growing demand for memory semiconductors with our continuously evolving advanced technological capabilities, product portfolio, and solid, quality customer base.

- This concludes my presentation.