Advantest Corporation

IR Technical Briefing

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IR Technical Briefing

Presentation Materials

IR Department Manager Yoshitake Kobayashi

Welcome to Advantest Corporation’s IR technical briefing. Thank you all for taking the time to be here. I’m Yoshitake Kobayashi, from the IR Department of the Corporate Planning Group, and I'll be your moderator today.

Our technical briefings are designed as deep dives into the technological and performance evolution of the semiconductors that we test, which affects demand for our products as much as growth in semiconductor production volumes. Exploring these connections can yield important insights about the market. Today, we’ll focus on high-end SoC devices and test technology. Let me introduce today's presenters.

First, Koichi Tsukui, Director and Executive Officer, CTO (Chief Technology Officer), and leader of our ATE Business Group.

Mr. Tsukui was involved in the development of measuring instruments, and later served as a sales representative in Japan and overseas, as well as general manager of the president's office. Currently, as the leader of the ATE business group, he directs the whole Group’s tester business, from research and development to customer support.

Next, Ralf Stoffels, a Senior Vice President at Advantest Europe, who is in charge of V93000 marketing within the SoC Test Business Unit.

Mr. Stoffels got his start in the semiconductor test business at HP in 1994, and has been involved with the V93000 from its initial ramp. He has held various leadership positions in marketing, and today he has world-wide responsibility for the V93000 platform as a Senior Vice President of Marketing at Advantest.

Today, Koichi and Ralf will give a presentation titled "Test Needs and Solutions in the High-End SoC Semiconductor Market." After that, we will take your questions. Go ahead, Koichi.

P3 **Agenda**

Koichi Tsukui

Good morning / afternoon. My name is Koichi Tsukui and I'm the CTO of Advantest. Thank

you very much for taking the time to attend our technical briefing today.

I will explain how the SoC test business has changed and how our R&D management is responding to these changes. And I will explain “Our Dynamic SoC test business” and how I have been working on R&D management. After that, Mr. Ralf Stoffels, Senior VP of Marketing for the V93000, will speak about the market environment for SoC semiconductors, future test needs related to high performance computing (HPC), which will drive the SoC test market in the future, and the solutions we provide.

P4 **Our Dynamic SoC Test Business**

Let's start with a look at the SoC test business environment.

P5 **Semiconductors Support Changing Lifestyles**

Semiconductors support global safety, security, and comfort. The use of semiconductors is expanding, and technological progress is making our lives more convenient and comfortable. Amid these changes, semiconductors are being used in more applications, and the demand for semiconductor test is increasing as the technology evolves.

Looking at the direction of technological evolution, in addition to the trend toward miniaturization of advanced-process devices, there is a trend called 2.5D/3D Scaling, intended to boost energy efficiency through improvements in circuit integration. All these changes in various semiconductor technologies, which we call “waves,” accelerate the difficulty and complexity of test. Next, I will explain the R&D management for capturing these “waves”.

P6 **R&D Management Initiatives from FY2018**

We maintain a high level of R&D investment as a driving force for value creation and social contribution. During the period of our second mid-term management plan, from FY2021 to FY2023, we plan to invest a total of 170 billion Japanese yen in R&D, an increase of 50 billion Japanese yen from the previous mid-term plan period. I'll briefly introduce our R&D management efforts since FY2018, when we launched our first mid-term management plan.

First, we've promoted R&D based on a long-term roadmap that takes its shape from semiconductor technology trends. We are striving to expand our platform strategy to a wider variety of customers and applications.

Secondly, we provide integrated test solutions. We are expanding our business domains from semiconductor mass production test to the design and evaluation and system level test processes, which are adjacent markets. We are also working to strengthen our test interface business.

Third, we are seeking to develop a test business that utilizes the cloud, software, and data

analytics. We have launched Advantest Cloud Solutions, a cloud service, and are working on commercialization with advanced semiconductor companies and partner companies that develop and provide solutions.

In addition to these three initiatives, we collaborate with leading customers and participate in industry consortia, and work to solve customer problems.

P7 **More R&D Synergies**

Next, I would like to introduce our R&D network. Our main R&D bases are located in Boeblingen, Germany, and Gunma Prefecture, Japan. About 30% of Advantest‘s total 6,500 employees are in R&D. Boeblingen mainly develops the V93000, and Gunma develops the T2000 and memory testers.

Previously, V93000 R&D and T2000 and memory tester R&D were separated, but in FY2018, we integrated them into a single organization, and global personnel rotations were implemented to speed up information sharing and development efficiency. I’m here in Boeblingen today, and we have about 600 employees here.

P8 **Today’s Focus : High-End SoC Test**

Whilst various “waves” of technological evolution in our business environment, today's focus is high-end SoC test. HPC devices, a market growing year by year, represent only a small fraction of all semiconductors, but their test intensity is much higher than other devices. Test technology requires not only measurement accuracy, but also technology such as thermal and power control. In response to these needs, in addition to our SoC tester platforms, we have strengthened our test interface and system level test with integrated solutions.

Ralf will now introduce our V93000 test solutions.

P9 **High Performance Computing (HPC) is the major driver of SoC Test**
Ralf Stoffels

Good afternoon, this is Ralf Stoffels and I will introduce our strategy and market performance in the area of HPC, which is one of the major drivers for SoC test and in that way very important for our corporate strategies.

P10 **Era of High-Performance Compute - Exascale Computing**

Let's take a look at the overall market. I have chosen a historical view here starting from the 1980s and it shows semiconductor revenue growth over that long period and in a very simplified way it connects the major growth waves with the technology which was introduced in each era. And when you look at the early dark blue phase it was the era of PC and internet, that drove the

first big growth of consumer computation, and then came the era of mobility which added a lot of capacity and equipment for the next big wave driven by mobile phone and mobile internet applications.

And I think we can clearly see what the next wave in this greenish color is going to be driven by. It is the era of HPC and the era of AI. And you can see clearly that the speed of innovation and growth have increased over time because each of those segments, of those technologies, have made it even more into the lives of everyday people, so while the era of PC was driven by commercial applications, only one family per PC, the era of mobility was driven by one phone per person, so the quantity went up significantly, so the coming era is even further driven by proliferation in almost every aspect of life and industry.

And you will later on see that there are other drivers as well, not just the volume, which drive the growth of that market.

P11 **Advantest V93000 led the way towards EXA Scale Computing**

And this is also a history of our own product line, and I'm just showing here the history of the V93000, the test system for SoCs, which actually got started with the era of the PC. So the V93000 was introduced in 1999, with the first generation we called Pin Scale, and this actually enabled us to serve the test requirements of the PC and the internet connected devices, and then as the next generation of devices came up, big SoCs driven by mobility, smartphones, we actually introduced Smart Scale, so like the smartphone, we actually addressed this with the Smart Scale generation. And that generation of the V93000 tester platform actually drove tremendous growth in the industry and of the product.

And just a bit more than a year ago we introduced EXA Scale. The EXA Scale generation adds the capabilities which are required to test the new upcoming supercomputers and AI engines. And most of my presentation here will deal with the challenges and the upcoming opportunities which this gives us by our position in the market.

And one of the reasons why we had such a successful growth of our platform was the ability to offer a compatible and upgradeable system and a path for our customers to go from one innovation to the next without having to change the essentials of the test programs and the investments they have made in the ATE(Automated Test Equipment). So we could always move our customers with very little effort from one generation to the next of their technology and from one generation to the next of our tester. And this is also the case for our new EXA Scale generation which seamlessly fits into that platform family. It was not only the compatibility but also the innovations we have driven during that time. So that brought us as shown here to 10K systems. That is just an estimation so of course it continues growing. We have probably already beyond that number.

P12 **Technology Leadership by continuous Innovation**

So the innovations I would also like to introduce to you here on this page we started already in 2000 as one of the first or THE first to address one Gb per second test speed for high-performance devices at a time when most of the other testers in the market were at far lower speeds. It was also essential that around 2005 we were the first to introduce an instrument with 160 amps of power supply, and we could add this to more than 1000 amps which was especially important for the big graphics chips arising at that point in time. I will talk later about what we expect the future is going to be in terms of power.

In 2012 that was also the time when the V93000 became part of Advantest and the Advantest platform strategy. We introduced the first card with 1.6Gbps on every channel. It was the fastest ATE on the market and also had the deepest scan capabilities, the most vector memory on the market. And this was complemented by high-speed cards which had an I/O capability of 16 Gbps. Also again the fastest in the market. And to an extent it is still the fastest today. And recently as I mentioned we introduced EXA Scale, which adds capabilities for the coming 5-10 years in terms of capabilities, speed, vector memory, and power. And with the new cards, it's 5000 which goes to 5 Gbps. We are offering a card which offers the headroom our customers need for development during the AI and HPC phase which I showed on the previous slides.

And the power supply is the other important thing in this era. We are talking about devices consuming 100s if not 1000s of amps of power, and with new power supplies, 256, we are offering that capability and a growth path to even more. Again this is all in one scalable and compatible platform family. So even innovations we have driven into the previous generation can be leveraged into the new one, and it is all compatible so our customers can easily move from one generation to the next without a break, and for our OSAT and contract manufacturing customers it is a way to preserve their investment in the previous generation, so that's a big factor for them to choose the V93000, because they can earn money continuously even after we have introduced the new platform generation.

P13 **Major Segments and ATE Customers**

With that I would also like to take a look into the technology changes and the market, before I talk about the technical innovations. We find for quite some time a market situation which is very much distributed into key players already. We segment the market into PCs and server CPUs, into PC graphics and into mobile APUs and modems. We use this segmentation because customers and also technology needs are different in these areas.

So let's briefly talk about PCs and CPUs. These are the classic players. Two big companies

serve that market, which are our customers. In PC graphics it's very much the same situation. Maybe two big drivers and a few very small ones. In mobile it is also the same. We are talking about 3-4 big players which serve the entire market of application processors and modems for mobile phones today. But it is very easy to foresee change here.

So let's look first at the upper segment, the PCs and server CPUs. So we find ourselves today in a situation where first, of course the existing players are still the strongest, the upper box here, the CPUs based on the Intel X86 architecture, but of course it is very visible today that new computing architectures are coming up, most prominently ARM, which is already in a very strong position in the market for several years now, and serving a lot of components into the internet and mobile devices and so on. There's also an upcoming new architecture called Risk 5 which is an open architecture and offers new opportunities. Definitely both can be seen as competition and an add-on to the classic X86 architecture. Also here we see a different way of segmenting, that's why I showed 2 boxes here. One is that we have the PC and servers driven by chipmakers, and we see a lot of them coming up, especially in China, a lot of startups arising right now, serving those processors, while on the other side and that is the second box, we also see many system builders, so the big hyperscalers in the industry doing their own processing engines, not only processing but also AI accelerators. They get integrated by those who in the end operate the servers, and that is basically their competitive advantages, to build chips exactly to their needs. It has a lot also to do with power consumption and efficiency, which is a key performance indicator in that market.

Let’s also take a look at the PC graphics. There is less of an architectural change. I think the big graphics players will stay the same but they will get new competitors, especially in China, because China is on its path towards independence from the traditional technology, and therefore there are a lot of startups which also engage in computer graphics, which is of course for us a new opportunity and a new market segment to serve.

Finally for the modems and APUs, we also notice a change towards more players, again China, and in two different business models. One is again the classic chipmakers who are serving chips to phone makers, but the phone makers start more and more to design and manufacture their own chips, and this is also a new development which leads to more growth, but also to a different set of requirements for the ATE. They require for example much more turnkey services. It's a very important development which we take into account for our strategies.

P14 **Major HPC Trends – Growing Complexity**

Having shown the changes in the market as such, let's also take a look at the technology moves. This is a very important view, although I need to carry you a bit into tech details, it is the

driver for innovation and it's the driver for why we invest into new versions and generations of our ATE.

Let's pick the six different ones and start with the upper left one, the integration. As I mentioned earlier, integration is going on, especially for the big servers, and as one means to do this, we see much more Chiplets, so multiple singulated chips onto one package, in one package, as the solution to grow the complexity as needed for those servers. That is also a very important fact for us as a test equipment vendor because it has new requirements for test. I mentioned already ARM CPUs here shown, which is mainly a source for new players, enabling new computer architectures, and it's a strong competition to the classical X86 architectures. On the complexity axis, you see that on the upper right, illustrated by this picture, we have with each major semiconductor generation change, node change, miniaturization change from i.e. 5 to 3, with each of those we also have new technologies coming in. For example, some of the big foundries would change their technology already for 3 nm from FinFET transistors to gate-all-around transistors, while others will do this in the 2 nm generation. It means failure simulation models they use to design test for those transistors are changing. It means there's a long period of time where a learning phase needs to be overcome, and for testing those or producing those technology nodes, and testing is the major tool for them to learn how to ramp the yields towards the next generation, and that is where test is fundamental helper, and test systems are being bought especially in those phases.

Other areas like on the lower part of this slide, like 3D packaging, increased complexity, like power and thermal, is driven by the fact that all this that I described before is happening at the same time, so more transistors, 3D packaging, and also the next nodes, are always driving for more power, and that is a big challenge not only in operation of the device, but also during test of the device, which means that we are very closely working with our customers to find solutions to test those supercomputer chips in their next generation. And then finally in the right lower corner, we have of course a lot of interconnecting problems. The larger a data center becomes, the more our customers are dealing with fabrics of data communication between the different computing engines, and that is to a big extent high-speed technology challenge, but it is also a power question. A lot of the power in today's data centers is used for the interconnects. Therefore, naturally the industry is looking for better solutions including optical connections. We of course are closely working with them to see what is the next big trend, I'll talk a bit about that, what are the challenges, and to what extent do we need to extend our solutions to test those kind of fabrics.

P15 **Growing Complexity drives Market Size for ATE**

Zoom in here a bit into the complexity of transistors. I said before it is not so much driven by

the sheer volume of devices, where we grow and the ATE needs to provide more testers, it is to a big extent driven by the complexity of the devices as well. And when you look at those different segments here, the growth of let's say the millions of transistors here, you see that the biggest driver per chip is the servers, CPU and GPU, while the next one is the client, that means the PC, and then the least of the drivers is still a super big driver, it's smartphone APUs. And in a very simple way you could say the test depends on the number of transistors. The more transistors the more test is required, because every transistor ideally gets tested, and that means the number of tests required and the time of test depends on the number of transistors. So that means that we need to always keep the equation in mind: number of devices tested times the number of transistors per device. That's a very good approximation of how much test is required.

And we see this. For the past several years, test times of individual devices went up significantly by maybe a factor of 100 in the last ten years, and we also notice that we have more tester insertions, so the device gets put many times on testers during the initial production phase of a device. For a long time, this was tackled by reducing data by compression, but it is very hard to achieve in the future, so therefore we expect test times will even further increase. Of course, in close cooperation with our customers, we try to reduce test time to make it always commercially viable solutions for our customers, but the big gains in terms of data compression are not to be expected in the future. We believe this gain will be on the number of tests required. This is of course driven by new failure mechanisms and 3D integration as well. Also, new methodologies need to come up and I will talk a bit about them. All in all, we can see with what I showed before and with this transistor model here, it is fair to believe that the increase of semiconductors projected from now until 2030 will also cause an equivalent growth in ATE as well. So, we believe that testing will track the growth of the semiconductor market, which I've shown on my initial slide.

P16 **Future Test Needs & Solutions**

So let's take a look into the challenges for ATE and what kinds of solutions we introduce and are envisioning for the future.

P17 **100x Complexity – Moore’s Law + 3D Integration**

I talked about complexity and I think it can be twofold, it can be the transistors as such, the type of transistors, the challenges with testing them, but also the sheer amount. Moore's Law more or less. And Moore's Law, together with stacking devices, I talked about Chiplets, here we see a picture of 3D stacked devices, our customers go into the third dimension, and this will increase the data volume to be tested by a factor of 100. This is easily foreseeable and it could

be even more. This requires testers to also use the technologies which our customers use, and with the V93000 we have chosen a path where we use the same way of integration in order to grow the capabilities of our tester without making it more expensive, in the same way.

You see here a picture of our test processor, an engine which we have in every resource of the testers. So, 1000s of these test processors in a system. The system is a very compact one, I think it is the smallest footprint in the industry. This is only possible because we use the same integration that our customers do. Here for example, the 2.5D integrated multi-core processor together with a memory. This device is developed by our own R&D, it is one of the core engines that power the growth and capabilities of the V93000. This is our latest generation, the EXA Scale. You see here that that way again we are the first and only ones so far who can on every channel of the system offer 5 Gbps, so the fastest in the industry, we also have the deepest vector memory, which is required by all that complexity to test those devices which are today coming up.

P18 **Power and Thermal beyond 1000W**

And I talked about power, and it is easy to imagine that those supercomputer devices, even though designed for consuming less and less power, by their complexity drive power requirements. We are talking here about 1000s of watts or 1000s of amps, current, which those device draw. Not only the current consumption as a static variable or static value is the challenge, but also the dynamics of power. Depending what kind of test is done, during the operation of those devices, what kind of load changes the devices have, the power can vary significantly, and the challenge is that this power gets controlled very rigidly. If the voltages of those devices change when the power changes, you can't be sure you really tested the device correctly, so during test it is one of the big challenges and requirements to keep the voltage stable while you change the power in huge steps.

Also, here we have chosen a technology which so far has not been deployed to test before. With the XPS 256, our new power supply, with the industry highest power integration, which has 256 amp per card, we can go far beyond 2000, even more amps in the system, and we can combine many channels to provide those high currents and this maximum power to the device. Not only that, we are first time using full digital control loops, which is again computing and performance digital architecture which we apply to our cards, enabling us to regulate the power faster than it can be done with a traditional analogy regulation circuit. With that come also some other advantages, i.e. we can protect the probe card of our customers from being destroyed by high currents. That is something you can only do if you have high computing power even in an analog card like a power supply for the devices.

P19 **Time To Market Challenge**

The other big challenge our customers have is test coverage. I mentioned already more test vectors, but there is also a new trend very visible: the devices, like it's shown here in this simplified picture of a computing engine, the devices are now dependent on software. Even during their early phases, even during test when they are not in their system yet. And they show a much more system-like behavior even when they are still on the wafer. Traditional ATE tests with digital inputs and gets digital outputs and is very much synchronized to the tester. We foresee and are entering an era where software even has to be loaded into the device at the test stage, which is a completely new way of approaching those complex systems. That requires innovation at the tester as well.

Traditional test architectures cannot deal with the fact that the device is driven by something unpredictable like software algorithms. Traditional scan technologies need to be augmented by new software-based technologies, so that doesn’t mean scan will be replaced, but it is an augmentation by new methodologies.

One of the new methodologies is to provide a link card to the device under test on the tester. We recently introduced the industry's first link scale cards. We call it Link Scale because it links to the device and can interact with it with native protocols and native ports like for example PCI express, used in PCs, or USB, like in many devices, mobile phones, being used as a wired interconnect. With this we are offering this industry-first card which goes, like every other instrument, on our test head, a very small form factor test head, and it actually offers functional test coverage on the tester, at a stage of the device where it is still on the wafer, for example. That way we can find failures before the device goes into the expensive package and it would cost a lot if we found these errors when they are already packaged. We moved test content towards probe, towards wafer sort, and also enable our customers for this card in the early stage of the design process to interact with the device much better than they could if they just had a normal test access like we had it for many years. Again, this will not replace today's test methodologies, but it will complement and add to those methodologies.

P20 **Summary**

With that I would like to summarize my speech here. We have seen the market has a lot of potential. This picture shows the semiconductor market, but it was also very clearly foreseeable that the ATE, the tester market would track this growth very much. We believe the tester market will grow by the same factors. As analysts say, we are seeing a semiconductor market of about $1 trillion by the year 2030, and as I said, we see this same percentage growth in that same period also for ATE. A lot of this will be driven by digital integration. Of course, there are other important areas as well but the major growth comes from computing engines, from integration

of digital structures into devices which drive the complexity for test.

I talked a bit about challenges and opportunities, and this 100x complexity growth is also one of the big driver engines. Of course, it is also the amount of devices being tested, but it is to a big extent also the complexity, which requires us to offer more and more clever ways of dealing with that. Also, the nature of the market is going to change, so like for example big system players who operate usually the data centers, are becoming system designers and even chip designers. They have different requirements than the classical ones, so we are talking here about turnkey test, which demands from us as a tester supplier to also change our ways of doing business with those customers. For them of course TTM becomes more and more a major challenge, because competition has gone up, so you have seen that on those pictures. And again, the way of doing this, we believe, can only be by evolving our systems the same way the market evolves.

So the V93000 did that for many years, you could see that we developed it with the leaders in this industry and for those leaders in the industry, and we always use very similar ways, because we believe in integration in silicon, so the more we can use the Moore's Law integration and 3D or 2.5D integration for packages, the more we can offer those innovations at a cost for our customers which actually makes sense for their cost measures. So also here we have proven this by being the market leader in this segment of computation. We have a major market share today and there are good signs that we can continue this because we are now again in the leading position. With EXA Scale that is basically a step into that next generation. We have chosen the name so we go with our Scale, Smart Scale and now EXA Scale, but EXA Scale also relates to the era of Exascale Computing, which is basically the driver for the growth but also the driver for a lot of challenges which we address with our technology.

With that I would like to thank you for your attention, and I am available to answer questions afterwards. Thank you.