Consumer Electronics Transform Chip Test Industry

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Innovative, sophisticated consumer electronics products have become the new major market for ICs, outpacing business and information technology markets in leading IC demand. The characteristics of the consumer market have affected the entire semiconductor industry supply chain, including the test equipment industry, and have put a new dynamic into play.

While cyclical demand, pricing pressures and technology improvements are not new to the semiconductor industry, the emergence of consumer electronics as the new major driver of the IC business has accelerated all these factors. This is not a temporary, cyclical change due to a market fad. Consumer electronics and mass-market applications for microchips are the future. Referring to Moore's Law, the SIA 2005 annual report says, " . . . this ability to cram an ever-increasing number of components onto a chip at constantly declining cost has revolutionized every aspect of human endeavor." This revolution will continue. With consumers as the main drivers of semiconductor demand, "better living through microchips" could be a universal slogan. IC-based living has become the norm as we enter the 21st century. We have only scratched the surface of what is to come – smart homes, smart cars, personal networks, telehealthcare, smart transportation systems. The stage is set for more widespread applications now that "everyman" is IC-habituated.

More, Faster, Cheaper

Consumers want reliability and quality but they are also extremely price-sensitive, fickle in their appetite for novelty and intent on sophisticated features. In the consumer world, product cycles are more compressed than ever before, while IC design and functionality become more complex. Downward pricing pressure is intense and unremitting. Expectations for fast, affordable, versatile consumer electronics require more complex devices that deliver more functionality, forcing the rate of change in IC design to keep pace with changing consumer tastes and demands. As the market becomes used to new and increasingly sophisticated products, product designers are challenged to create new-generation versions more quickly. No one can completely predict where the creativity of product designers or the tastes of consumers will lead us, but the technology innovation bar is being raised faster and higher than ever before.

Challenges to Traditional Test

The new marketplace realities present a number of challenges to traditional test:

1) Device product cycles continue to shrink, leaving much less time for program development and debug.
2) Device complexity is accelerating, increasing requirements for test expertise in multiple areas.
3) Product segments converge quickly in the face of rapid innovation, reducing the opportunity to recover investments.
4) ATE is challenged to keep pace with increasing device performance requiring higher R&D budgets.
5) New tester platform introductions present significant costs and risks to both IC manufacturers and ATE vendors.
6) Collaboration is critical in order to devise innovative test solutions rapidly. The industry must make the shift from industrial mindset to knowledge-based mindset.
7) Given the increasing trend toward specialized and customized devices, no single vendor can meet all manufacturers' needs
8) Test providers, as well as semiconductor manufacturers, have to broaden their supply/demand models to encompass the larger, global marketplace to understand how to better balance their business models between innovation and the need to protect margins for technology reinvestment. One way to do this is to look at ATE costs more broadly, as part of the wider business context.

Moore's Law vs. ASP

Moore's law states that transistor density on ICs doubles about every two years. The increased density of transistors, coupled with increased speed, permits chip designers to readily address the consumer demand for electronic products with higher performance offered at decreasing prices. ATE capital spending has more than kept pace with the economics resulting from Moore's Law. On a per-transistor basis, ATE capital spending is approaching one nano-dollar per transistor (see Figure 1).

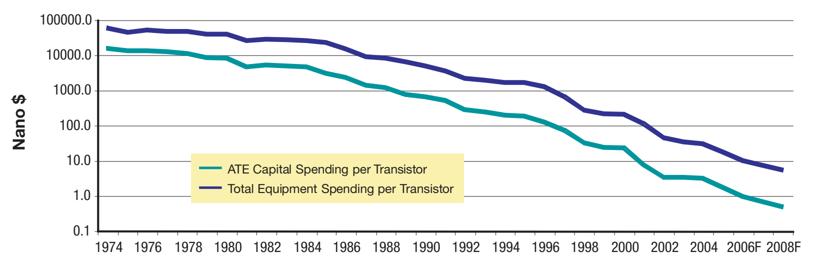

Figure 1. Capital Spending Per Transistor Produced
Data: VLSI Research, Inc.

However, chip makers don't sell transistors, they sell complete IC units. Therefore, it is critical to look at the cost of ATE on a per-unit basis and to do so in the context of IC average selling prices (ASP). A historical look at SoC ATE Capital Cost per IC unit data shows a clear trend of increasing costs using a three-year rolling depreciation cycle. Even excluding the 2000-2001 bubble and burst, there has been a gradual increase in SoC ATE spending per IC unit over the last 15 years. Similarly, the spending per unit as a percent of ASP has gradually increased as well, again excluding the 2000-2001 spike (see Figure 2).

Shrinking Margins vs. the Cutting Edge

While this -2 percent contribution by test to IC gross margins from 1989 to 2005 may seem minor, the upward trend in ATE cost per unit is the larger concern to chip makers. Leading-edge semiconductor designs targeted for consumers result in more device complexity and diversity, and traditional high-performance test systems cannot scale down test costs as readily or rapidly as the price of the chips they must test. The semiconductor equipment industry thus finds itself in a quandary: the need to accelerate development of state-of-the-art testers and simultaneously lower test cost.

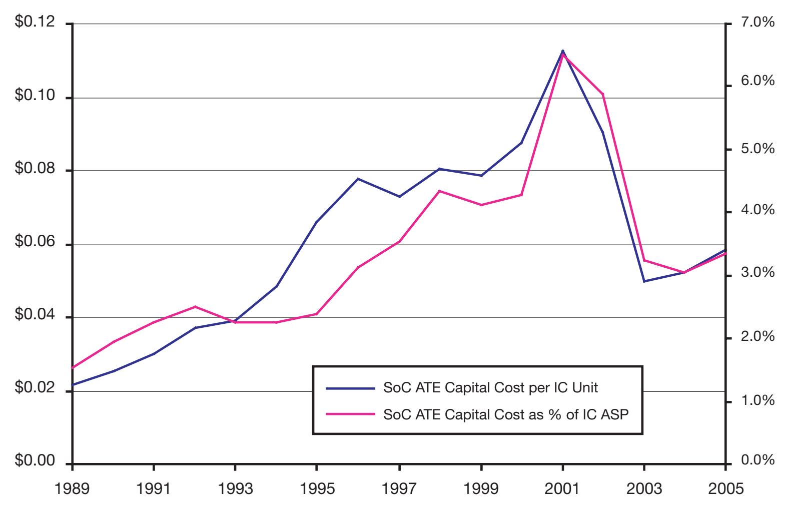

Figure 2. IC ATE CAPITAL COST (SoC ATE 3-Yr Depreciation Cost per IC and Cost as % of IC ASP). Data: VLSI Research, Inc.

In fact it can be argued that the traditional level of R&D funding for the test industry at large is in jeopardy given the relentless downward price pressure of consumer demand. The traditional model of a proprietary tester designed to test a limited number of device types no longer works, especially for highly integrated semiconductors required to meet dynamic consumer market needs at prices that are affordable.

Open Architecture Industry and Standards

For the semiconductor test equipment industry, as the traditional business model appears increasingly less viable, what then is the alternative? In 2002 the nonprofit Semiconductor Test Consortium (STC) was formed by a group of semiconductor, equipment and instrumentation companies – now numbering more than 80 companies, individuals and universities – to develop a common test architecture that is open, documented and solutions-oriented with test instrument modules available from multiple suppliers in support of semiconductor manufacturers. In 2004, the STC successfully yielded such an open architecture by publishing the OPENSTAR® hardware and software specifications. During that time, Advantest launched the T2000 SoC test platform based on these specifications, which has met great success to date. In 2005 the first independent third-party vendor developed and shipped production OPENSTAR-compliant modules.

The work of the Semiconductor Test Consortium supports the entire semiconductor industry because it provides an appropriate, workable forum to respond to the evolutionary changes in the industry. The concept of an open test architecture is a sea change for the test industry, as well as for the semiconductor industry – a radical departure from the traditions that have prevailed for decades. But although radically new, it reflects and responds to the industry's current reality.

Chip Makers and Equipment Suppliers Benefit

A healthy industry yields benefit for all major participants. Open architecture test specifications must meet this criterion to become the industry norm. The benefits of open architecture to chip makers may seem more apparent perhaps than those to test equipment suppliers. For semiconductor manufacturers, the most profound benefit of an open test standard is lower total cost of test. Test system lifetime is extended through upgrades with future products from multiple suppliers. Frequent change-over to next-generation, proprietary, closed test systems for new, leading-edge devices is eliminated, significantly reducing chip makers' depreciation expenses. With the introduction of open architecture test, the average SoC ATE life span should be extended from three years to perhaps 10 years or more. If this extension is translated into a conservative estimate of 2 percent (YoY) less SoC ATE capital expenditures against VLSI Research's forecast, and 10-year depreciation cycles are applied, the increasing cost per IC unit trend can be reversed (see Figure 3).

Assumptions

1. Assumed 8.6 percent CAGR for IC units. This is equivalent to applying a 10-year CAGR to the VLSI data IC unit data and forecast.
2. Assumes 7.7 percent CAGR of SoC ATE sales which is equivalent to applying a 10-year CAGR to the VLSI non-memory test sales data and forecast.

Furthermore, an open, common test platform maximizes test equipment uti- >>

>> lization, increases factory efficiency, and lowers training, software development, factory integration, hardware and corporate integration costs. And finally, multiple test suppliers for a standard platform ensure new test products are developed to meet time to market and production ramp schedules for new semiconductor devices.

However, test equipment suppliers also benefit from the evolution to open test specifications. As with chip makers, the primary benefit of a collaborative test industry is lower cost. Test vendors lower R&D costs and minimize investment risk when products are co-developed with other suppliers. In an open test architecture world, test suppliers also co-develop test products directly with chip makers. Test equipment companies become free to focus their investment on their core competencies and collaborate with other industry experts to add incremental products to an open, industry-standard platform.

Co-Creating the Best Test

In the last few years, accelerated marketplace dynamics have winnowed the number of industry test players, both primary and supporting. In this dynamic evolution, more creative problem solving is needed for those who want to remain as industry players, which points to a more collegial way of developing solutions. One of the resulting changes of the new, contemporary industry business model has been a shift from cutthroat competition to collaboration. To meet the rapid-fire challenges of the new market dynamics as well as to stay vital, semiconductor companies must partner as they never have before, up, down and across the supply chain. The pacesetters are doing just this, with the formation of the STC as the first step.

Beyond the quid pro quo division of labor of a cooperative effort, collaboration means that everyone, chip makers and equipment suppliers, is invested – literally and figuratively – in a generative process that is focused on developing the best products. The definition of "best" will change as market dynamics change, but certainly state-of-the-art technology, precision engineering, high quality and cost will be key factors.

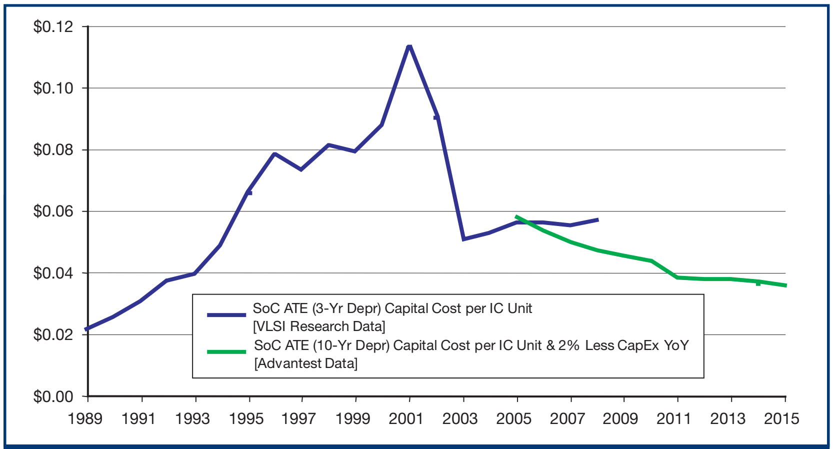

Figure 3. IC ATE CAPITAL COST (SoC ATE Depreciation Cost per IC, $US)
Data: VLSI Research, Inc.

The strategic alliances of the past were primarily marketing agreements. The new order of collaboration involves creating value-added products and services.

From Hardware and Features to Knowledge and Business Savvy

In this new order, ATE companies must widen their approach from a focus on hardware and proprietary platforms to an emphasis on added value. Extendable high-performance test systems are a must. Undeniably, systems that deliver high throughput, reliability, maximum uptime and all other test essentials are key to maintaining high test standards.

But in the new semiconductor industry framework, additional qualities will contribute to competitive advantage, both an ATE company's and its customer's. Test engineering talent, knowledge and experience are the human capital building blocks of added value. But, as critically important is a company's willingness to develop the best solutions, whether by reconfiguring core competencies or by adding needed competencies, and a company's astuteness in managing its own business, whether by protecting margins for R&D reinvestment or by having an infrastructure capable of keeping up with the fluctuations and split-second timing of mass-market demands. ATE companies must be able to contribute as value-added partners, not just equipment suppliers.

For an ATE company to be successful in this century it must make a shift in problem solving that follows the shift in the industry. Success requires a willingness to do things differently, clearsightedness about strengths and weaknesses, scrutiny rather than mere observation and a willingness to work collaboratively across the industry for the mutual advantage and continuous evolution of technology. In terms of the health of the industry, in a truly collaborative environment, everyone wins.

References

1 Figures 1& 2: "VLSI Research Executive Advisory: Cost of Test - Big Driver in ATE"; May 13, 2005.
2 Figure 3: STC Global Openstar® Conference keynote speech, March 6, 2006, by Risto Puhakka, VLSI Research Inc. ■

About the Author

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President and CEO of Advantest America, Inc., R. Keith Lee is a technology industry veteran of more than 25 years. Since joining Advantest America in 1984, he has held senior management positions in design and development, sales and marketing, and applications and systems engineering. Before Advantest, he worked for Megatest Corporation, Mitel Corporation and AT&T in senior marketing management and engineering positions. He holds a bachelor's degree in electrical engineering from Auburn University.