Modern SoC Handlers With Advanced Technology Lower Test Cost of Ownership

Handlers, especially pick-and-place handlers used for testing of today's complex SoC packages, are playing an increasingly important role in test cost of ownership (CoO).

IC features such as built-in self-test (BIST) and design for test (DFT), and test system features such as increased parallelism continue to improve throughput and CoO of automatic test equipment (ATE) by reducing test time. But, thanks to advanced technology the handler can also play a defining role in determining the throughput and CoO of the test cell. While other ATE companies partner with, or more recently, acquire handler companies, for decades Advantest has designed and manufactured its own handlers as well as test systems, resulting in singular insight about optimized handler performance and its benefits.

The Importance of Handlers in CoO Modeling

An accurate CoO model is critical in assessing test cell cost of ownership, but typically the focus is on the test system. Handler unit-per-hour curves, utilization and jam rates are also important factors in figuring CoO. If they are not included or are included incorrectly, poor decisions in equipment selection and capacity planning can result.

As Figure 1 shows, CoO can be calculated as the sum of capital expenditures plus operating expenditures divided by good throughput.

$$CoO_N = \frac{CapEx_N + OpEx_N}{UseableThroughput_N} + LossEx_N$$

Figure 1. Cost of Ownership Equation

Capital expenses can be calculated by depreciating the base price of the equipment plus any upgrades and peripherals over the cell lifetime, and operating expenses should include the time required of all personnel (test engineers as well as equipment operators). Throughput is calculated by multiplying the good units per hour by the utilization by the uptime of the equipment (see Figure 2). Every percent increase in throughput that is achieved results in a percent decrease in the $/unit.

Handler Performance Improvements

To understand how the performance of pick-and-place handlers – and, correspondingly, throughput and overall test cell CoO – can be improved, it's useful to know the basics of how handlers work: 1) an operator loads devices into the input tray, 2) the handler moves devices into a carrier where they are brought to the appropriate temperature for testing, 3) devices are placed into the test socket, tested and placed back into the carrier, and 4) devices are sorted based on the test results and are placed in separate output trays. Throughput is restricted by the speed of the package handler that moves the DUT into and out of the ATE, but increases in parallel handling capability in state-of-the-art machines have somewhat ameliorated this.

In addition to these stages of the handling process, another consideration in

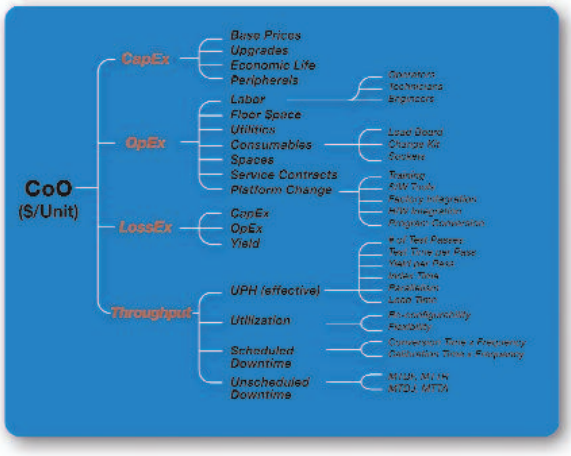

Figure 2. Exploded View of CoO Model, Including Role of Handler

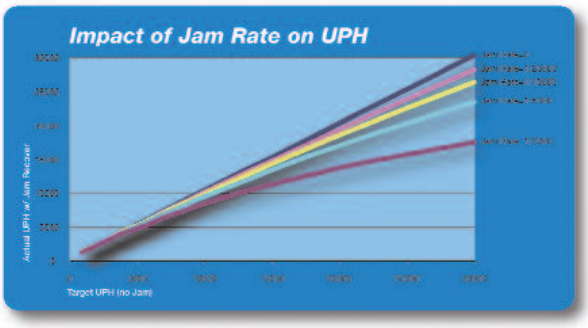

Figure 3. Impact of Jam Rate on UPH

calculating throughput is index time, which refers to the amount of time needed to remove tested devices from sockets and install new devices.

Improved handler performance is not only about increasing handling speed but also about increasing the speed without damaging parts. Along with this, achieving repeatable low contact resistance in the socket is required.

State-of-the-art handlers have improved the speed with which devices can be moved from tray to socket and back to tray while avoiding damage to delicate devices, and some also feature an innovative electro-pneumatic "soft-touch" air pressure control system that uses software to precisely set the contact pressure on the package. The adjustment allows repeatability of socket contact and less damage to tiny, lightweight devices.

The latest generation of handlers also employs a new vision alignment system for the accurate positioning needed by less than 0.4 mm-width fine pitch devices configured in high-density IC packages, including chip-scale and quad-flat packages (CSPs and QFPs) and ball-grid arrays (BGAs). Optical precision placement helps avoid jams that shut down the test cell for manual clearing.

The throughput of vision-alignment handlers is excellent, exceeding 4,000 units per hour for simultaneous testing of four devices and ensuring rapid time to market.

Improved Utilization Yields Better Throughput

Utilization is also important in evaluating the impact of the handler on test cell throughput. As parallelism is increased and cycle times are reduced, the number of test cells tends to decrease, with the result that fewer cells have a proportionately greater impact on utilization. Lot sizes, package type mixtures and temperature test requirements can also wreak havoc on utilization, and therefore on throughput and CoO, because of higher consumable cost associated with higher parallelism load-board assemblies and change kits.

The way to maintain high utilization among fewer test cells is a handler with flexibility. One way a handler can provide increased flexibility is through easy changeover of the handler DUT layout unit. The ability to expand or contract the number of test sites in parallel can allow smaller lots to be run with lower consumable costs associated with load-board assemblies and change kits. The cost of change kits has been reduced because new kits have fewer parts, costing less even than those for previous generations of handlers with less parallelism.

Temperature also offers flexibility. A high throughput handler equipped with tri-temp (rather than bi-temp) capability is better suited for a factory's inconsistent device mix, resulting in higher equipment utilization. The small cost premium paid for tri-temp capability is offset by the utilization gain and capital reduction.

Uptime Counts in Figuring Performance

Uptime should also be considered when evaluating handler performance. The key metric is mean time between jams (MTBJ), which is typically measured in terms of the average number of devices that are handled between jams. Previous generations of handlers typically jammed an average of once per 10,000 pieces. With new test cells capable of testing 20,000 to 25,000 units per hour, such rates are clearly unacceptable (see Figure 3). Another important metric is mean time to assist (MTTA), the amount of time required to clear a jam. Difficult jam cases require the operator to partially disassemble the handler, which can take up to an hour.

Conclusion

To be effective in reducing the cost of SoC testing, semiconductor manufacturers need to assess the performance of their handlers and ensure their cost models include this critical part of the test cell. Very recently, technological innovations have made handlers the most promising area for realizing additional, substantial savings and a reduction in the cost of ownership of the test cell.

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Toshio Maruyama
President and CEO
Advantest Corporation

R. Keith Lee
President and CEO
Advantest America Corporation

Japan
Advantest Corporation
Shin-Marunouchi Center Building,
1-6-2, Marunouchi, Chiyoda-ku,
Tokyo 100-0005, Japan

Phone +81-3-3214-7500
Fax +81-3-3214-7705
www.advantest.co.jp/en-index.shtml

North America
Advantest America Corporation
3201 Scott Blvd.
Santa Clara, CA

Phone 408-988-7700
Fax 408-987-0680
info@advantest.com
www.advantest.com