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Advantest Corporation IR Technical Briefing

Characteristics and Needs of HPC/AI Device Test

November 28th, 2024

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NOTE

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Agenda

- ✓ Business Environment of SoC testers
- ✓ Characteristics and Needs of HPC/AI Device Test

Business Environment of SoC testers

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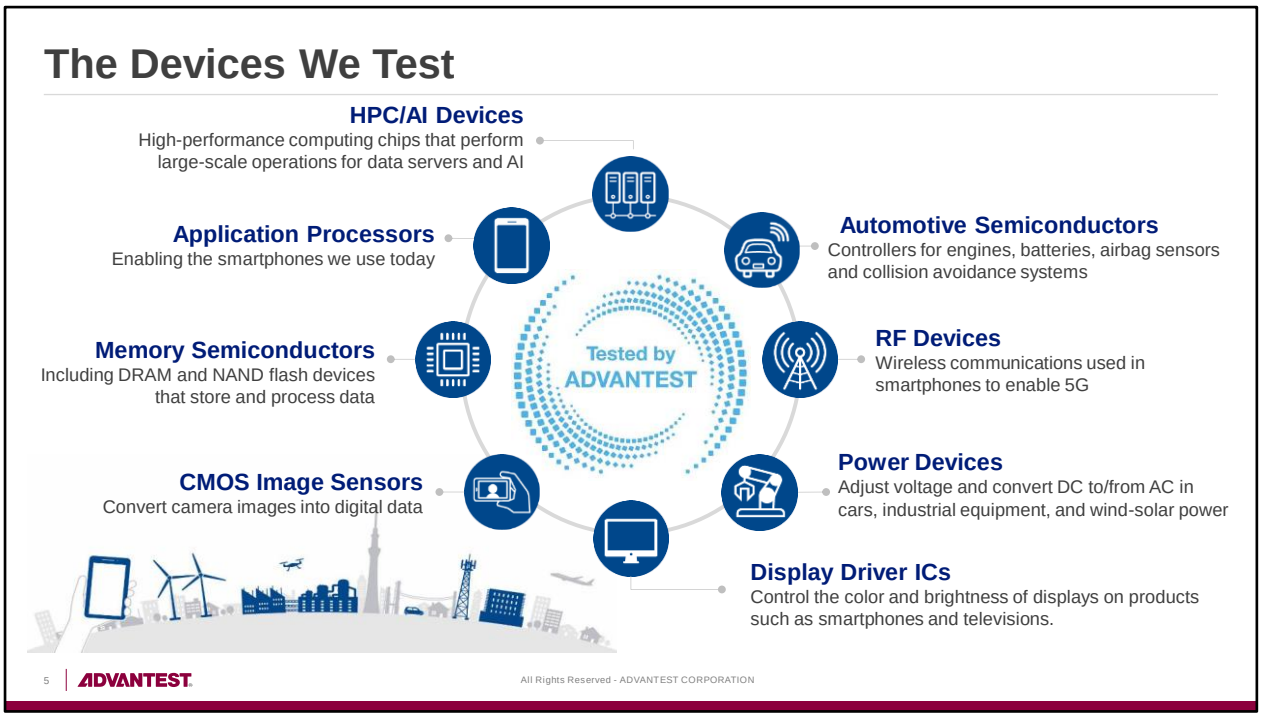
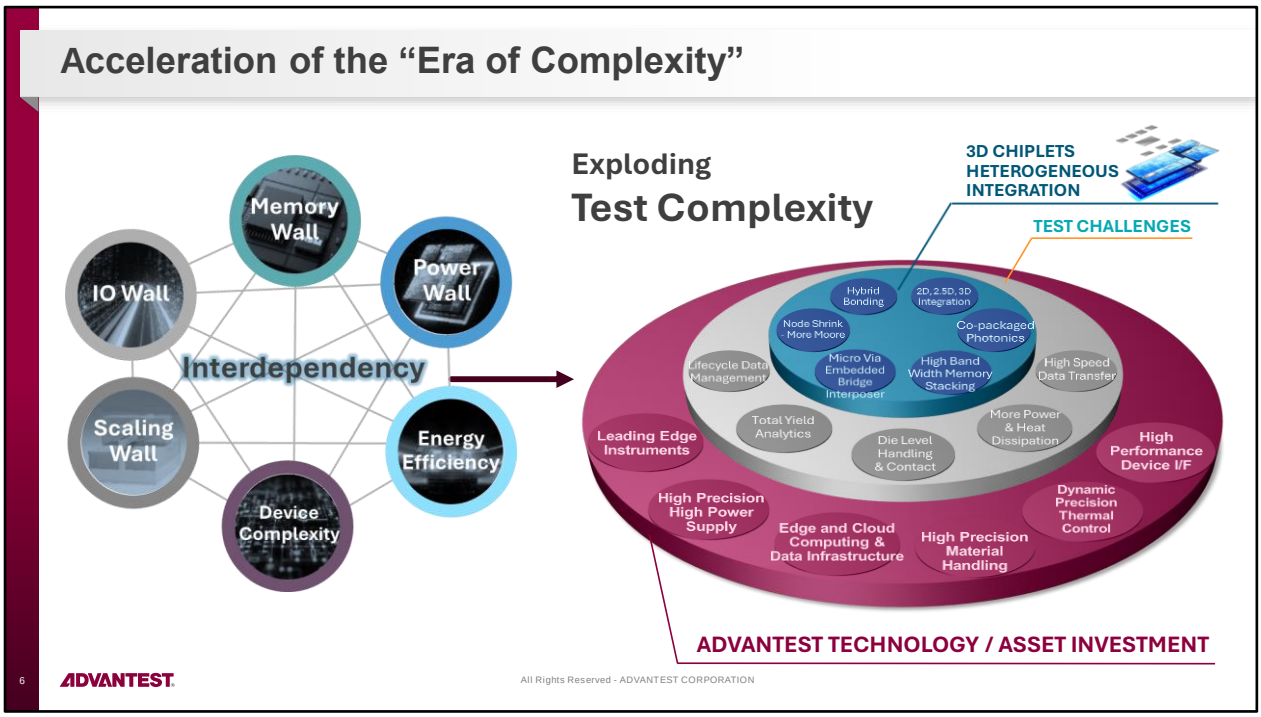
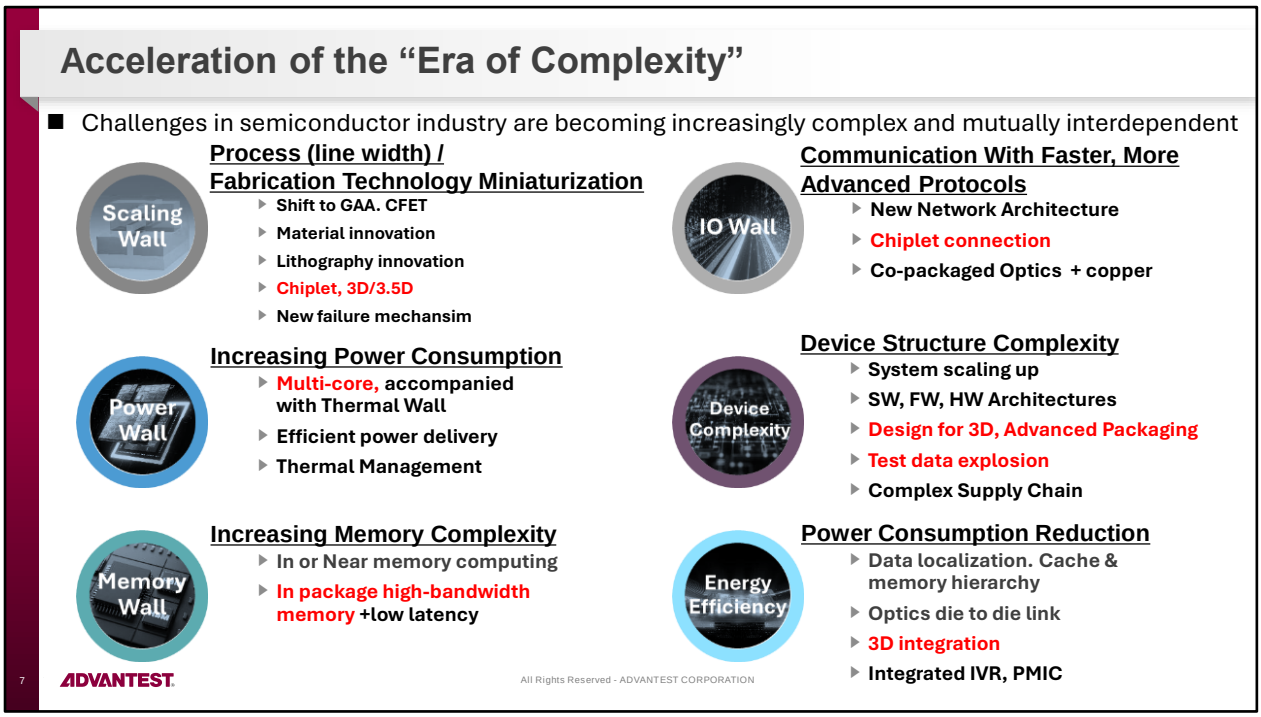
- Hello. My name is Akio Osawa.
- Let me quickly introduce myself. I joined Advantest in 1989 and was assigned to the S.E. Department, which stands for Systems Engineering. Since then, I have mainly worked as a SoC tester System Engineer, promoting testers, providing test solutions to customers' test issues, and providing technical support.
- I currently oversee a global department called System Solutions, which is responsible for system and application engineering for all testers, including memory as well as SoC.
- I will explain about the business environment surrounding SoC testers.



- Advantest plays a role in supporting the quality of all semiconductors through testing.
- From smartphones and other devices to data center infrastructure, semiconductors are now used in all kinds of applications. The technological advancements in semiconductors, such as the addition of various functions and improvements in energy efficiency to enable long-term use of devices without recharging, have enhanced the convenience of our lives today.
- In recent years, AI technologies that efficiently collect, learn, infer, and generate large amounts of data with high efficiency have been emerging. With AI becoming a pervasive force in our daily lives, it is essential to enhance the processing power of semiconductors to create an environment that can process dramatically increasing amounts of data at higher speeds. Currently, new semiconductor packaging technologies are rapidly advancing the heterogenous integration and performance improvement of high-performance semiconductors such as HPC and HBM.
- As a system engineer during my tenure at Advantest, I have long been working closely with customers who develop and evaluate various semiconductors. The role of an SE is to contribute to the customers' time to market, time to quality, and time to volume through technical support. Specifically, we support the optimization of the test environment for each device by providing support for the development of test programs and working with the customer to identify defective areas of the semiconductor. I have listened to their technology challenges and explored enhancements of test solution requirements. I would, then, provide feedback to our R&D team to develop next-generation test solutions. I have experienced such cycle numerous times.
- Today, we will focus on HPC. Later on in this presentation, Iino will explain in detail about the characteristics of the technological advancement associated with these semiconductors and the test needs they are creating.



- In our presentation of the Third Mid-Term Management Plan announced in June of this year, we stated that “the semiconductor industry is shifting into an era of complexity.”
- The challenges in the semiconductor industry can be summarized as shown on the left side of the slide, where the six circles representing the challenges are all inter-connected. This means that each of these challenges is significant and inter-related in terms of complexity.
- Furthermore, complexity has a multiplier effect. For devices responsible for advanced computing such as for AI, the interdependence between these challenges becomes even stronger.
- In the semiconductor process, the test process is essential for solving interrelated problems. In the ‘era of complexity,’ the more the interdependence between issues increases, the more it is necessary to strengthen, advance, and integrate test solutions. In other words, test intensity increases.
- The diagram on the right shows the value which advanced test solutions provide.
- With the proliferation of AI, the semiconductor value chain is tackling the challenge of integrating advanced computing functions such as learning, inference, and generation into a single device.
- In this process, many interdependence challenges have already become apparent. Going forward, we anticipate that these will become even bigger industry challenges. In response to this trend, we are confident that the technology assets and know-how we have cultivated will increase in value even further.



- Let’s take a more detailed look into the challenges which the semiconductor industry faces. Let me outline the detail of the challenges in the six circles.

    - **Scaling Wall**: Process (line width) / Fabrication Technology Miniaturization
    - **Power Wall**: Increasing Power Consumption
    - **Memory Wall**: Increasing Memory Complexity
    - **IO Wall**: Communication With Faster, More Advanced Protocol
    - **Device Complexity**: Device Structure Complexity
    - **Energy Efficiency**: Power Consumption Reduction

  Among these, the items highlighted in red, are prominent challenges in these several years.

- As I explained earlier, these challenges are becoming more advanced while being mutually interdependent and interdisciplinary.

- In today's presentation, we will lay out the characteristics and test needs of HPC/AI devices. In doing so, we will explain how these challenges are leading to the increase in test volumes for HPC/AI devices.

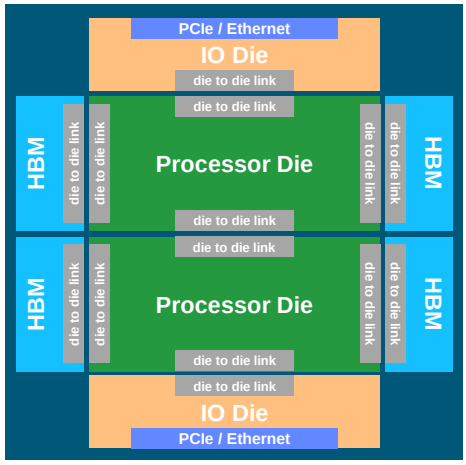
- Now, I will hand the presentation over to Iino-san.

Characteristics and Needs of HPC/AI Device Test

ADVANTEST

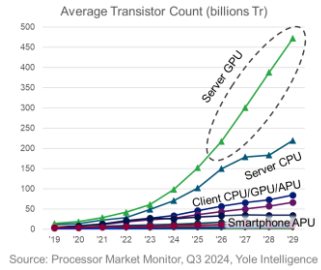
- Hello. I am Takashi Iino.
- From here, in my presentation titled 'Characteristics and Testing Needs of HPC/AI Device Test,' I will explain the testing needs of HPC/AI devices, including the technical background.
- I joined Advantest in 2001 and have been supporting our domestic and international customers with SoC device test technology ever since.
- Currently, I belong to the Center of Expertise under the marketing organization for the SoC tester “V93000,” and I am supporting customers in solving their problems from a technological perspective through development of test technologies in the high-performance digital domain.
- In the following slides, I will introduce the characteristics and technological trends of HPC/AI devices.

Characteristics and Technical Trends of HPC/AI Device



Source: Advantest

- Characteristics
  - Chiplet design
  - Multiple processor dies
  - Multiple IO dies
  - Multiple HBM
- Trends
  - Miniaturization, new process technology, 3D Assembly, Increase in package size
  - Chiplet and multi-die integration to be the industry standard
  - Further increase in the bandwidth of IO dies (PCIe5/6, multi-level transmission)
  - HBM with higher speed, increased complexity, and further increase in stacking



Source: Processor Market Monitor, Q3 2024, Yole Intelligence

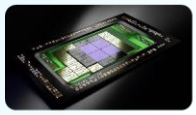
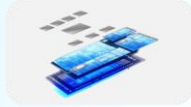
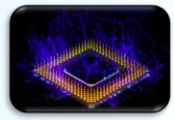
Multiple large dies are integrated and must be efficiently tested in a short period of time

- The large block diagram on the left represents processors operating in data center AI servers. It is mainly composed of processor dies, IO dies, and High Bandwidth Memory (HBM).
- Common features of HPC/AI devices include chiplet design, multiple processor dies, multiple IO dies, and multiple HBM.
- As a recent change, cryptocurrency technology emerged around 2014. In response, ASIC mining and GPU technology were developed rapidly, and parallel computing capabilities gained traction.
- At the end of 2022, OpenAI's GPT-3 and ChatGPT were introduced, bringing generative AI technology to the public. While further advancements and expansions of advanced AI technologies are anticipated, achieving this will require computational capabilities far exceeding current levels.
- As such, the required processing power is increasing year by year. To keep up with this, technology trends such as new process technologies, larger, faster, and more complex packaging are emerging. Consequently, as indicated by the chart showing average transistor count by product category in the upper right on this slide, the number of transistors in server GPUs could potentially increase fivefold over the next five years compared to current levels.
- There are many challenges in test technology for volume production of HPC/AI devices. Among these, the most significant challenges are related to test volume and test time.

Structural Factors Contributing to HPC/AI Test Volume Increase

Performance Assurance Enhancement

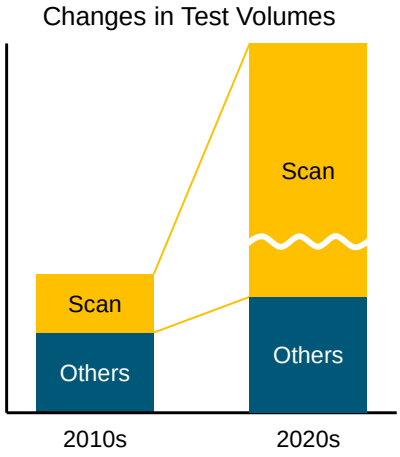
Longer Test Time, Test Patterns Increase | Test Process Increase

Process (line width)/ Fabrication Technology Miniaturization	New process Technology	Device structure Complexity Multi-Die Integration	Power Consumption Heat Dissipation Increase	High Quality Assurance
				
Transistor Count Increase	Failure Models Increase	Wafer Test : Verification of Die Characteristics Package Test : Full Inspection of Assembled Dies	Prevention of overheating/burnout Optimization of test time/test flow i.e., thermal control	Die Level Test Burn-In at multiple temperature settings System Level Test

Advancement of HPC/AI semiconductor technology demands better quality and performance assurance

- Now, let me walk through the testing challenges caused by the advancement of HPC/AI devices. This slide shows five major technology trends and the associated test challenges as well as their impacts on test processes. These can be categorized into longer test time and/or increase in test processes.
- First, the process nodes miniaturization. For products that adopt cutting-edge process nodes, the number of integrated transistors increases dramatically, requiring a vast number of test patterns to ensure their quality compared to the past.
- Next, the new process technology. The evolution of transistor architecture continues to support miniaturization. FinFET technology has become widespread, and recently, Gate All Around (GAA) is being introduced. Furthermore, a new architecture called Complementary FET (CFET) is being proposed for sub-2nm processes. The miniaturization and innovation of transistor architecture are likely to trigger new failure modes that did not exist before, necessitating additional test patterns to detect them.
- Third, the multi-die integration. To maximize yield, the quality and individual characteristics of each die are examined before packaging. In some cases, dies with similar performance and characteristics are considered for inclusion in the same package. Then, after packaging, it is necessary to reconfirm that all these dies function correctly.
- The increase in the number of transistors and dies also leads to thermal control challenges. During volume production, in order to carry out tests efficiently, a large number of transistors have to be run in parallel per unit time. As a result, a large current continuously flows through the device, and this manifests as heat generation. Heat energy changes in proportion to the square of the current, as expressed by P=RI^2. Therefore, it is necessary to consider and optimize the trade-off between heat generation and test time in order to prevent incidents such as burning from overheating.
- Lastly, high quality assurance. In data centers, tens of thousands of devices operate in clusters. If even one device fails or experiences performance degradation in the field, it can significantly impact overall performance. Therefore, it is essential to ship devices that have been tested under stress conditions with high coverage to ensure very high quality.

Expanding Test Content and Increasing Scan Volume



- 2010s
  - DC test
  - BIST [1] test including SRAM and high-speed interface etc.
  - Functional test
  - Scan test

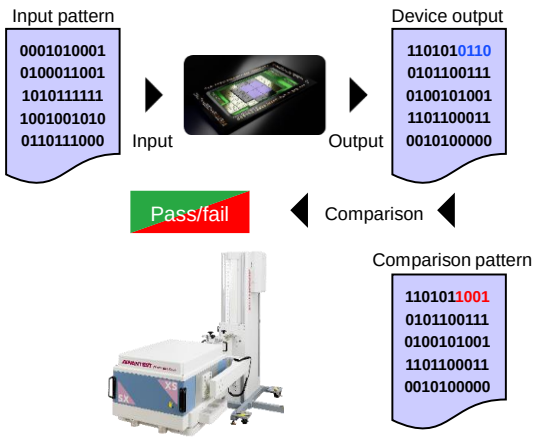
  [1] Built In Self Test (BIST) ：Test-dedicated circuits designed within the device for testability
- 2020s
  - Basic test items are largely unchanged
  - DC test slightly increased with increasing pin counts
  - BIST test growth due to enhanced device functionality

Exponential increase in the number of transistors caused an explosive growth in scan test volume

- In order to efficiently test whether the hundreds of millions of transistors integrated into a device are performing correctly, a test method called "scan test" has been used for SoC devices. The features of the scan test will be explained in the following slide.
- Before that, let me explain about the changes in scan test volume. As illustrated in the chart on the left, there have been significant changes in volume and test time for large-scale device test, especially between the 2010s and the recent 2020s. The increase in scan test volume has been a major driver of this change.
- In the 2010s, in addition to DC test and BIST test, scan test was also performed, but the proportion of scan test was not that significant.
- Entering the 2020s, however, the proportion of scan tests has significantly increased, and this trend continues until today. While the increasing complexity of devices has also caused an increase in other test items such as DC test, their growth rate is not as substantial as that of scan test.
- EDA companies have developed pattern compression technologies to improve the transistor test rate per unit time. Although new efforts to further enhance efficiency are actively ongoing, the reality is that they still cannot keep up with the increase in the number of integrated transistors.
- Scan test remains the most efficient method for testing exponentially increasing transistors, and its volume is exploding.
- In order to reduce the increase in test time, customers, EDA companies, and ATE vendors are also conducting various research and development activities. EDA companies have proposed solutions to improve scan test efficiency, such as networked scan circuits and scan-over-HSIO technology that uses high-speed IFs such as PCIe and USB as scan input/output pins, to which Advantest is also involved in joint technology development. Depending on the results, the growth rate of scan test volume may change in the future.

Test and Characteristics of HPC/AI Devices

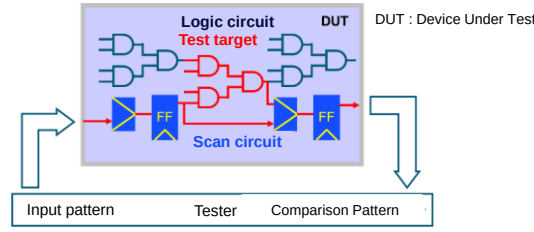
HPC/AI Devices Logic Testing



Scan test

- Typical item of DFT (Design for Testability)
- Main test item for SoC devices from the 2000s to the present

- Scan circuits are inserted in the device to arbitrarily set conditions of the sites to be measured
- Generate test patterns based on assumed failure models and locations
- High efficiency /high test coverage (95 to 99.5%)



Increasing transistor count causing lengthening of "test patterns" = Lengthening of test time

- Now, let me explain how SoC testers measure devices in the context of HPC/AI device test and their characteristics.

- The left side of the slide outlines the process for HPC/AI devices logic testing. Signals are input into the device, and after various processes are performed within the device, the output signals are received by the tester. These signals are then compared to pre-set comparison patterns to determine whether the device performs as intended.

- Generally, the input patterns and comparison patterns used in test are automatically generated by EDA tools, which are used during a semiconductor design phase, based on the device specifications and test specifications.

- On the right side of this slide, we have described the scan test which I have referred to earlier. A scan test is a standard test item that emerged based on a concept called design for testability. First proposed around 1990, scan test has continued to evolve and is now a major test item for SoC devices.

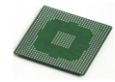
- A key feature is the insertion of a test circuit called a 'scan circuit' into the device circuit. With a scan circuit, conditions of specific areas to be tested can be set arbitrarily, and the outcome after running a test can be checked. Using this mechanism, EDA tools generate test patterns that incorporate target transistor areas and simulate failure models.

- Then, if the number of transistors were to double, and if the performance efficiency of scan patterns also doubled, it would be possible to maintain the same test time as before.

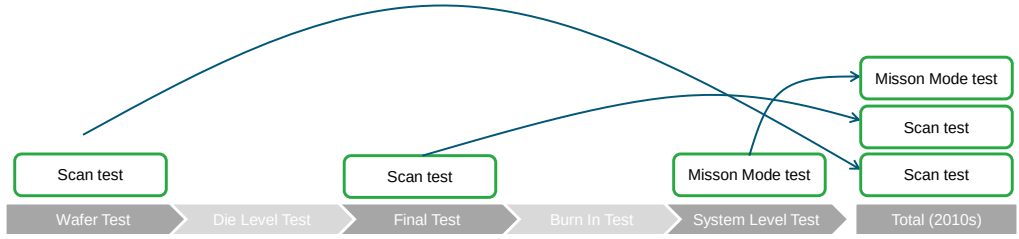
- However, as of now, the efficiency of pattern generation algorithms has plateaued, and there are limits to the parallelization of scan circuits. As a result, the lengthening of "test patterns" due to the increase in the number of transistors continues. This is a major factor leading to longer test times.

Test in the 2010s: Screening of Defective Devices

- ✓ Wafer Test：test each die individually,　Final test：test each packaged die individually
- ✓ Test Volume：Wafer Test ≒ Final Test（Package Test）
- ✓ Test items optimized for front-end and back-end processes, respectively
- ✓ System level test is added depending on the application



Note: The height of the boxes in the image does not correspond to the test times for each test

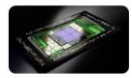


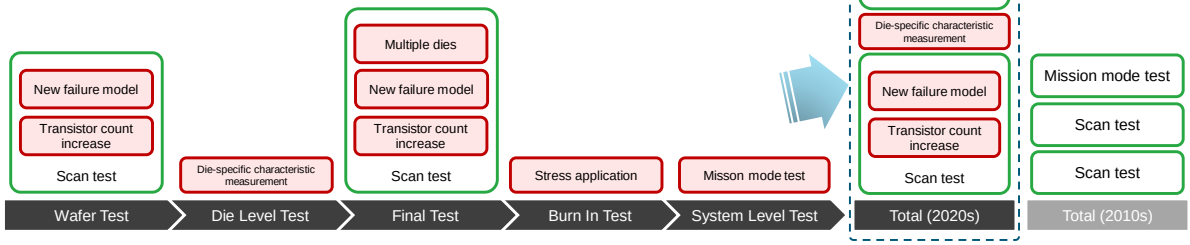
- I explained that the test volume has significantly increased in the 2020s compared to the 2010s. In this slide and the next slide, I will delve a bit deeper into what has changed.
- First, let me review tests of the 2010s. The slide title "Screening of defective devices" refers to the primary purpose of test which remains to this day. However, compared to the present day, test in the 2010s was simpler.
- The chart at the bottom of the slide represents typical test processes and main test contents. In the wafer test, which is carried out in the front-end, a scan test is first performed. After the device is packaged, a final test is carried out. Here, a scan test of similar nature is conducted.
- In reality, the test items that were performed in wafer test and package test are different. However, as a result of selecting and carrying out the most optimal test items, there was no significant difference in the test volume.
- Furthermore, for certain devices, system level test was inserted to further enhance test quality.
- To clearly visualize the total test volume of the test process, the main test items are stacked on the far right.

Test in the 2020s: More Complex, Longer Test Time

Note1: The height of the boxes in the image does not correspond to the test times for each test.
Note2: Items in the red boxes are factors driving demand growth in the 2020s.

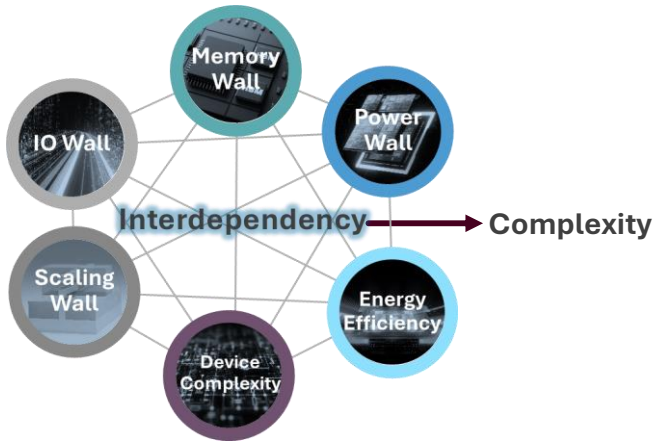
- ✓ An increase in scan test volume due to increased number of transistors and new failure models
- ✓ Additional test insertions for die-specific characteristic measurement and an increase in test contents in final test due to multi-die assembly
- ✓ Increased efforts to further ensure high quality, including multi-temperature test, burn-in, and system level test

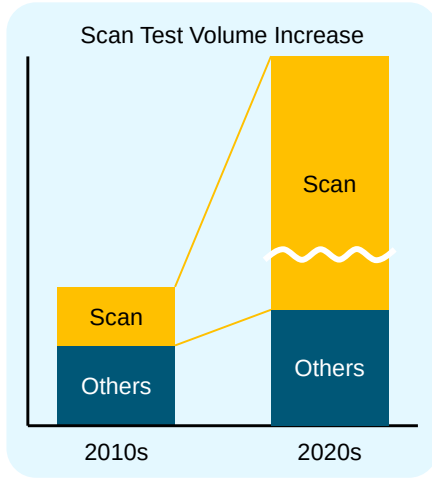




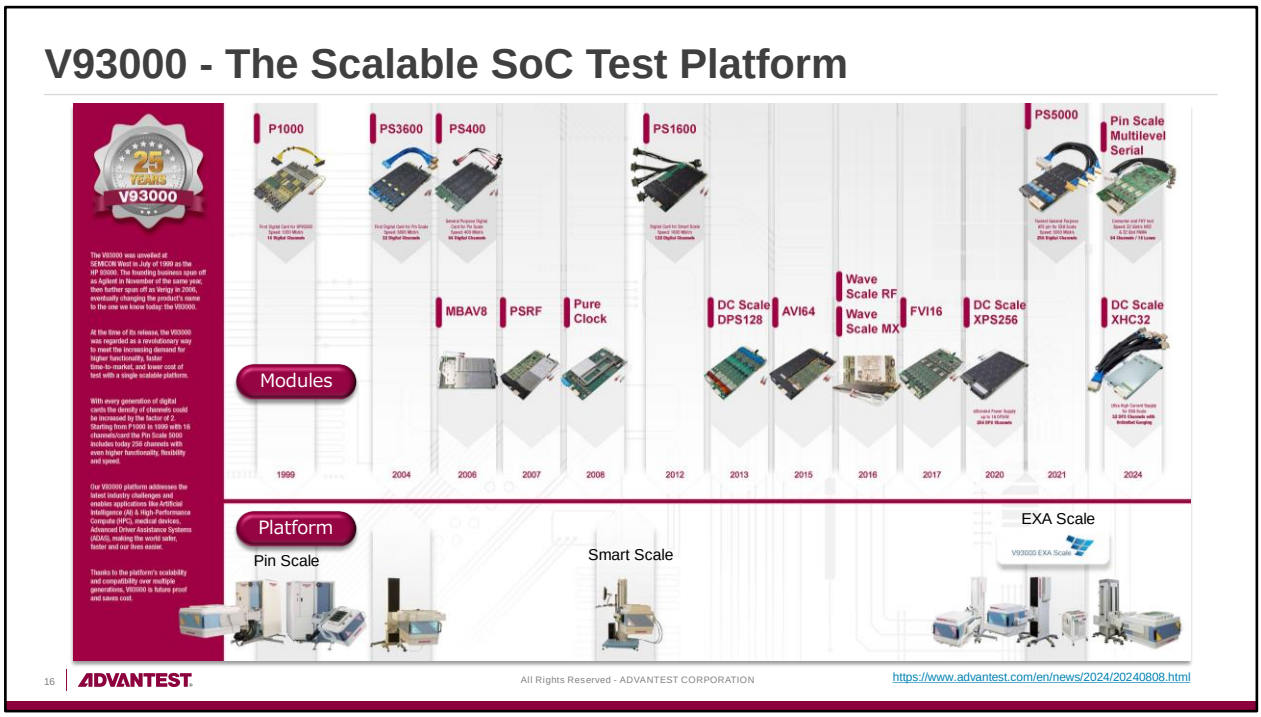
- How has test evolved in the 2020s? The test contents has grown in both complexity and test time.
- First, for wafer test, the volume of scan test has increased due to migration to new process nodes and the increase in the number of integrated transistors.
- The trend is similar for final test. However, the volume of scan tests increases even more to test the multiple dies assembled in a package.
- Furthermore, an additional process called die level test is being considered to more accurately determine the individual characteristics of each die. Although similar test items have been performed during wafer test in the past and are still being performed today, there is an ongoing active discussion about inserting an additional process to test the dies individually after dicing, due to several reasons including heat generation issues.
- For devices such as automotive that conventionally face high reliability requirement, tests such as burn-in which apply high thermal stress and mission mode test have been performed. Recently, for similar reasons, stress application has also been implemented for HPC/AI devices, and mission mode test has become a requirement for the most part.
- Lastly, we have stacked the test items to compare with the 2010s as in the previous slide. Please note that the height of each box does not accurately represent the test volume. However, you may still get an idea of the significant increase in test volume compared to the 2010s.

Test Demand Driven by Accelerating “Complexity”





- Up to this point, we have broken down the factors contributing to the increase in test volume for HPC/AI devices and explained the reasons behind them. This slide serves as a summary.
- The performance improvements in HPC/AI devices are bringing numerous technological and test challenges. These challenges are intricately linked and interdependent, as shown in the diagram on the left.
- Moreover, the number of transistors integrated within a single package continues to increase with miniaturization, new process technologies, and multi-die assembly. To efficiently test the vast number of transistors, scan test is increasingly utilized, and as shown in the chart on the right, their volume continues to grow significantly.
- As part of the AI technology roadmap, the goal over the next decade is to achieve Artificial General Intelligence (AGI) capable of handling a wide range of tasks like a human. To this end, HPC/AI devices will continue to evolve in terms of data processing capabilities, communication speeds, and energy efficiency, leading to even more test challenges than we face today.
- In response, we will continue to listen to the latest technical challenges faced by our customers and explore test technologies. We will feed these back to our R&D to create next-generation test solutions.



- Finally, let me touch on our SoC tester business.
- This slide shows the 25-year evolution of our flagship SoC tester, 'V93000.' Starting in 1999, during the era of personal computers, V93000 met the test demands of PCs and internet-related devices with the Pin Scale platform. The next generation, Smart Scale, increased its presence in the SoC market driven by mobility/smartphones. In 2020, we introduced the latest platform, EXA Scale, which is now supporting the HPC/AI era.
- Currently, we hold nearly a 60% share of the SoC tester market and recognize our position as a leader in the field of high performance computing. There are three core competencies behind the company's No 1 market share.
- The first competence is the "strong relationships with HPC customers, nurtured through 20 years of communication." By keeping abreast of customer technology trends and requirements in a timely manner, we have continued to provide speed, accuracy, density and performance that are one step ahead of the rest.
- The second competence is our test platform that combines scalability and compatibility. When transitioning to next-generation devices, our customers can upgrade the necessary measurement modules to enhance the value of their existing platforms and continue to utilize them. Furthermore, our platform offers compatibility that allows for the smooth transition of existing assets, such as test programs, to the new platform.
- Finally, our global engineering support capability is our third competence. Our engineers are optimally positioned against the globally disaggregated semiconductor supply chain. We provide a high level of engineering support required by our customers, working together on a global basis.
- These have enabled us to share a long-term roadmap with our customers and maintain a virtuous cycle in which we continue to develop and supply the test solutions required for the new generation of devices in a timely manner.
- While embodying the core competence of our SoC tester business, we have been supporting the world's leading customers advance their semiconductors. We are excited to continue to work closely with our customers facing increasing complexity and to expand our test solutions.

- This concludes my presentation. Thank you for listening.