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Advantest Corporation IR Technical Briefing

Characteristics and Needs of HPC/AI Device Test

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Agenda

- ✓ Business Environment of SoC testers
- ✓ Characteristics and Needs of HPC/AI Device Test

Business Environment of SoC testers

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The Devices We Test

HPC/AI Devices
High-performance computing chips that perform large-scale operations for data servers and AI

Application Processors
Enabling the smartphones we use today

Memory Semiconductors
Including DRAM and NAND flash devices that store and process data

CMOS Image Sensors
Convert camera images into digital data

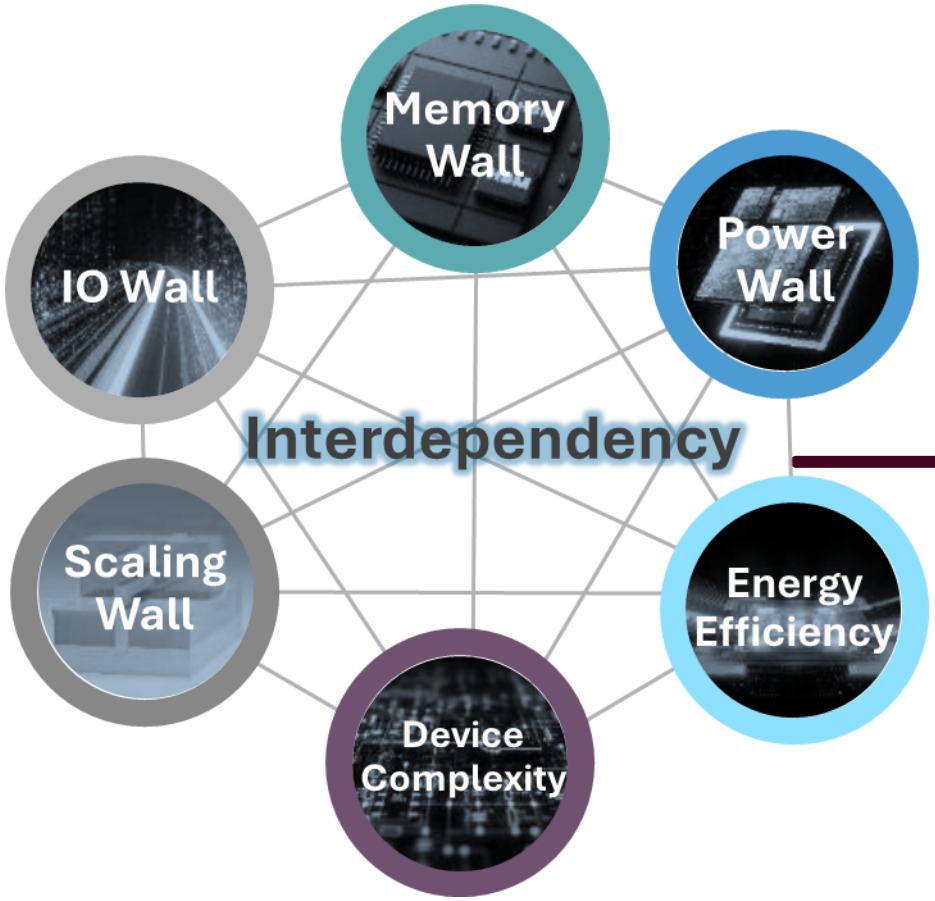
Automotive Semiconductors
Controllers for engines, batteries, airbag sensors and collision avoidance systems

RF Devices
Wireless communications used in smartphones to enable 5G

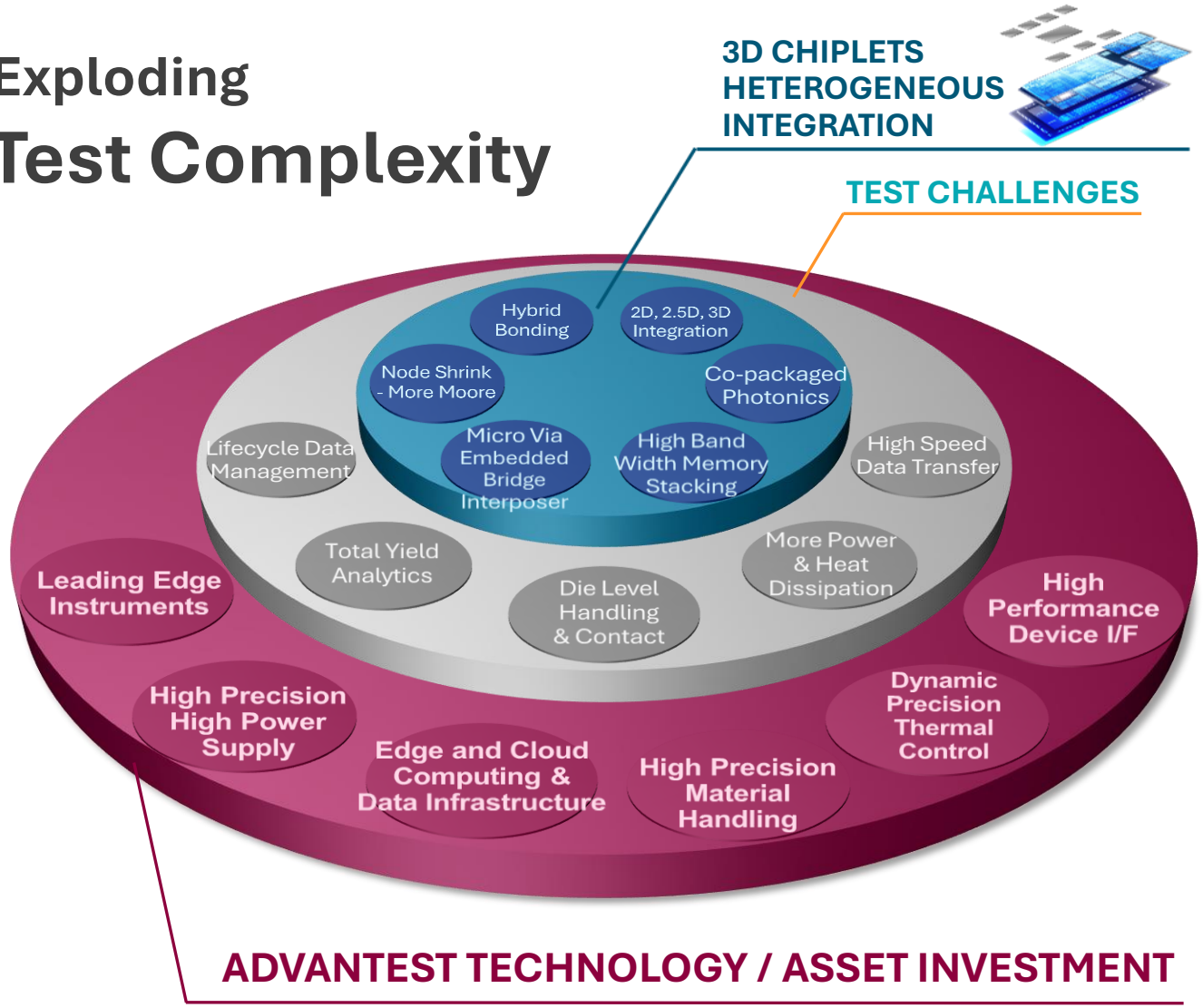
Power Devices
Adjust voltage and convert DC to/from AC in cars, industrial equipment, and wind-solar power

Display Driver ICs
Control the color and brightness of displays on products such as smartphones and televisions.

Acceleration of the “Era of Complexity”



Exploding Test Complexity



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Acceleration of the “Era of Complexity”

- Challenges in semiconductor industry are becoming increasingly complex and mutually interdependent

Process (line width) / Fabrication Technology Miniaturization

- Shift to GAA. CFET
- Material innovation
- Lithography innovation
- Chiplet, 3D/3.5D
- New failure mechansim

Communication With Faster, More Advanced Protocols

- New Network Architecture
- Chiplet connection
- Co-packaged Optics + copper

Increasing Power Consumption

- Multi-core, accompanied with Thermal Wall
- Efficient power delivery
- Thermal Management

Device Structure Complexity

- System scaling up
- SW, FW, HW Architectures
- Design for 3D, Advanced Packaging
- Test data explosion
- Complex Supply Chain

Increasing Memory Complexity

- In or Near memory computing
- In package high-bandwidth memory +low latency

Power Consumption Reduction

- Data localization. Cache & memory hierarchy
- Optics die to die link
- 3D integration
- Integrated IVR, PMIC

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Characteristics and Needs of HPC/AI Device Test

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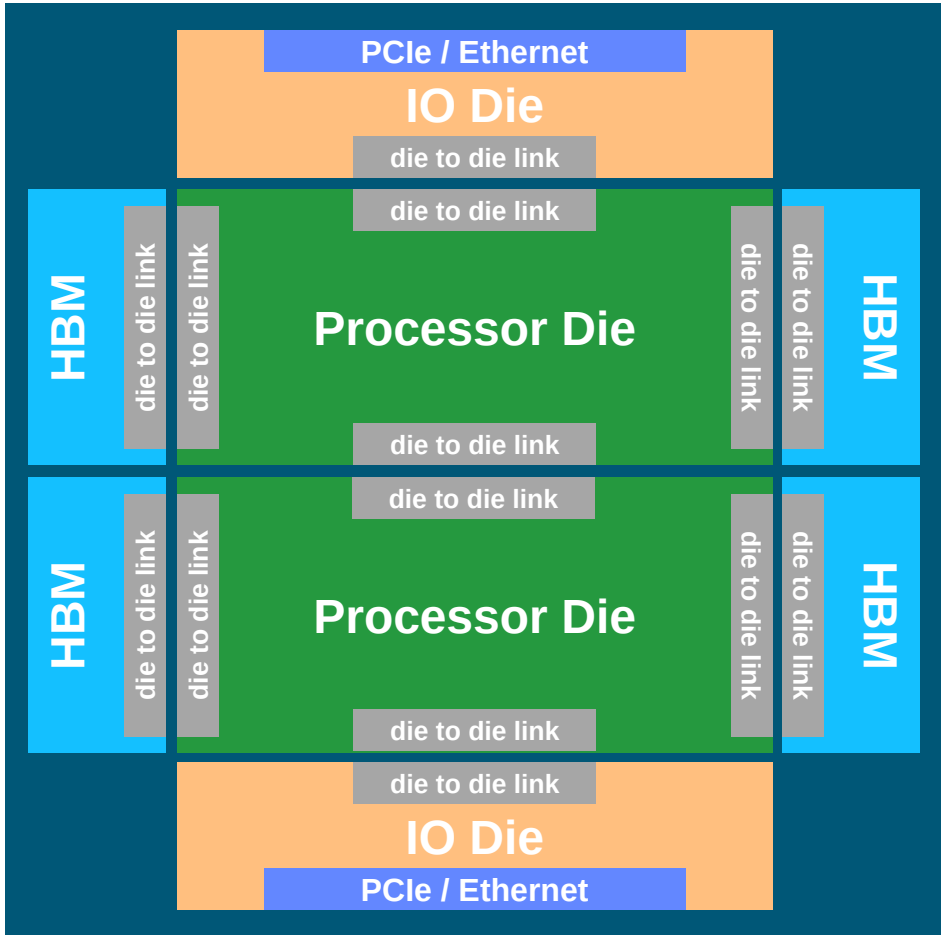
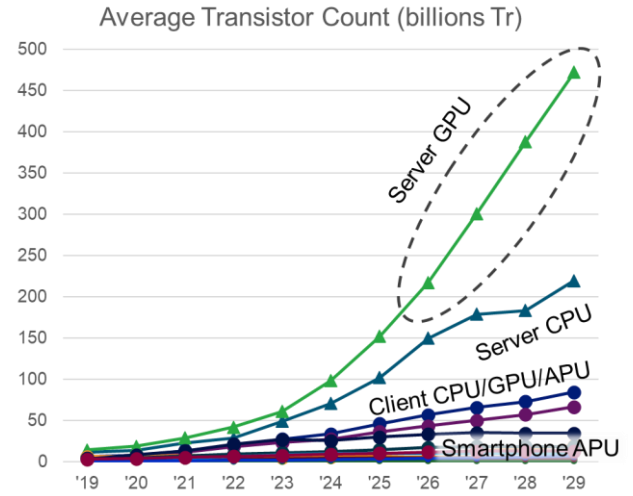
Characteristics and Technical Trends of HPC/AI Device



Source: Advantest

- Characteristics
  - Chiplet design
  - Multiple processor dies
  - Multiple IO dies
  - Multiple HBM
- Trends
  - Miniaturization, new process technology, 3D Assembly, Increase in package size
  - Chiplet and multi-die integration to be the industry standard
  - Further increase in the bandwidth of IO dies （PCIe5/6, multi-level transmission）
  - HBM with higher speed, increased complexity, and further increase in stacking



Source: Processor Market Monitor, Q3 2024, Yole Intelligence

Multiple large dies are integrated and must be efficiently tested in a short period of time

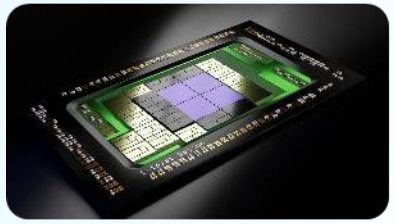
Structural Factors Contributing to HPC/AI Test Volume Increase

Performance Assurance Enhancement

Longer Test Time, Test Patterns Increase

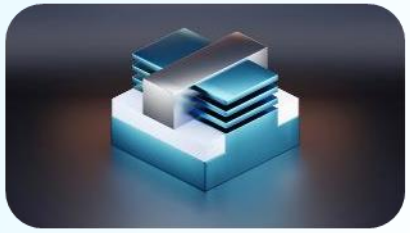
Test Process Increase

Process (line width)/ Fabrication Technology Miniaturization



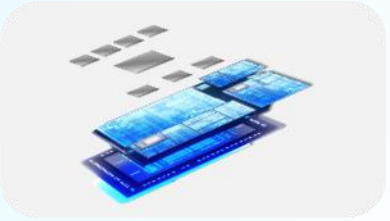
Transistor Count Increase

New process Technology



Failure Models Increase

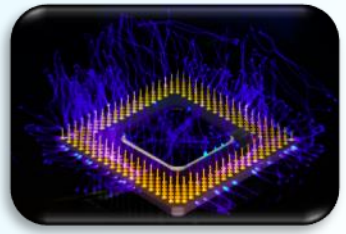
Device structure Complexity Multi-Die Integration



Wafer Test：
Verification of Die Characteristics

Package Test：
Full Inspection of Assembled Dies

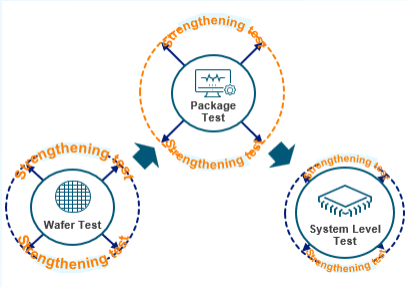
Power Consumption Heat Dissipation Increase



Prevention of overheating/burnout

Optimization of test time/test flow i.e., thermal control

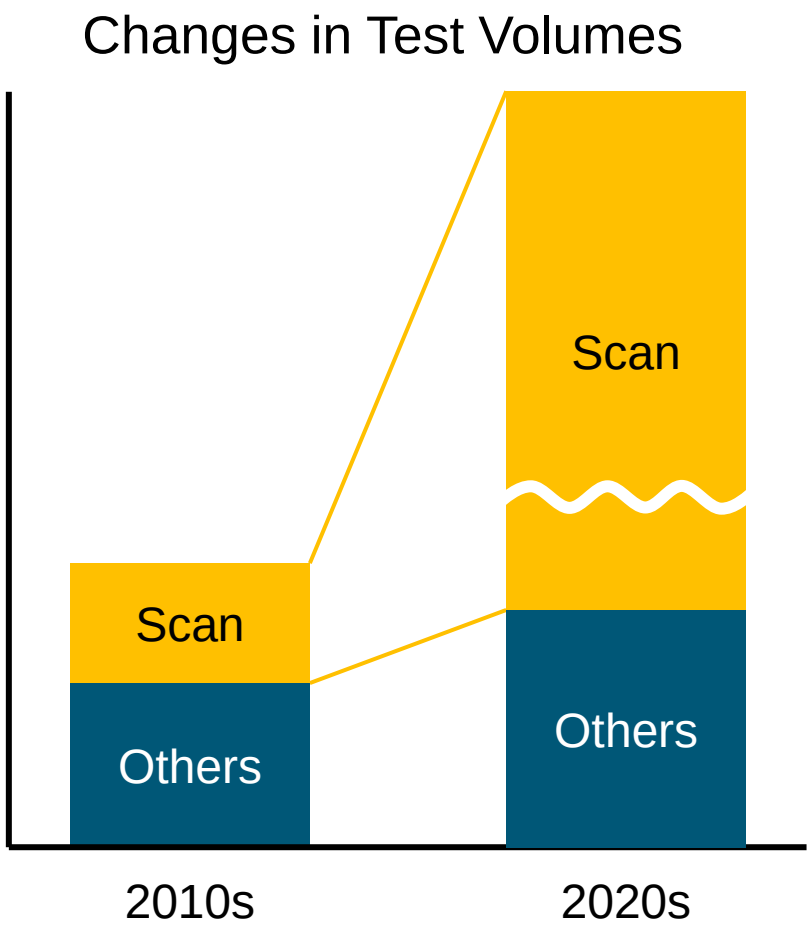
High Quality Assurance



Die Level Test
Burn-In at multiple temperature settings
System Level Test

Advancement of HPC/AI semiconductor technology demands better quality and performance assurance

Expanding Test Content and Increasing Scan Volume



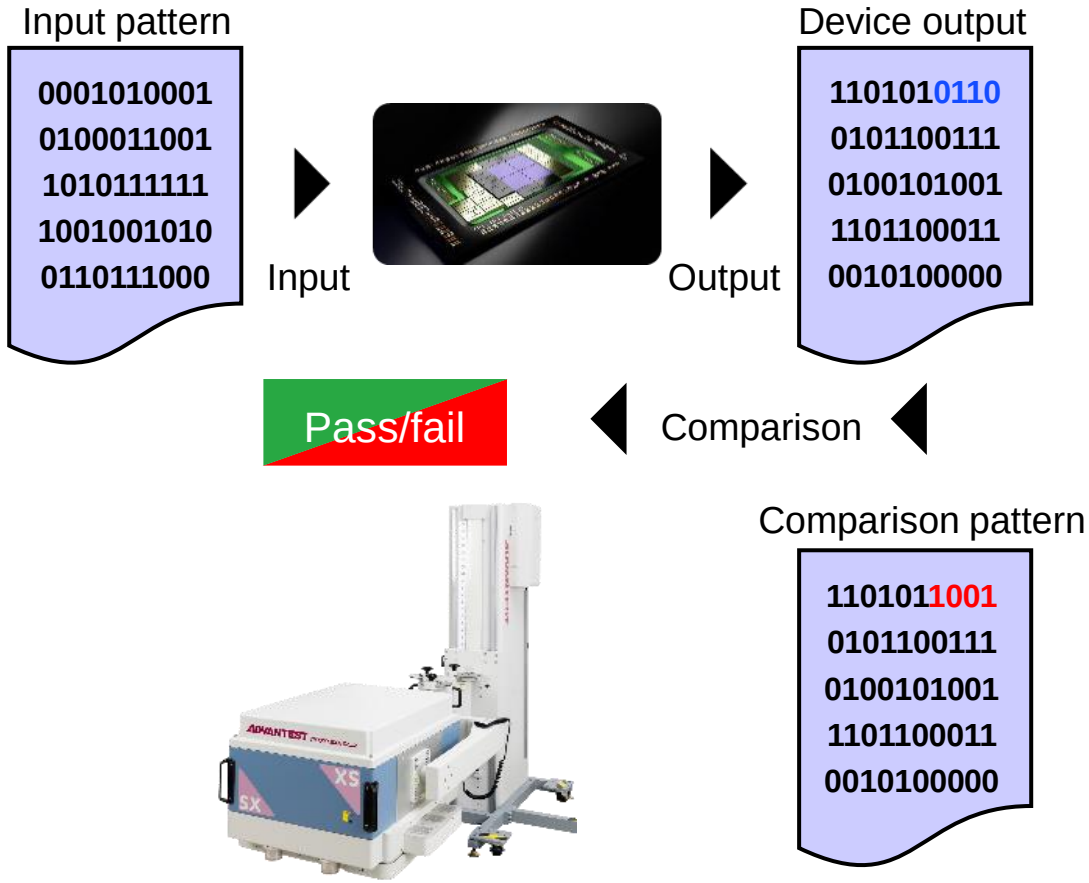
- 2010s
  - DC test
  - BIST [1] test including SRAM and high-speed interface etc.
  - Functional test
  - Scan test

  [1] Built In Self Test (BIST) ：Test-dedicated circuits designed within the device for testability
- 2020s
  - Basic test items are largely unchanged
  - DC test slightly increased with increasing pin counts
  - BIST test growth due to enhanced device functionality

Exponential increase in the number of transistors caused an explosive growth in scan test volume

Test and Characteristics of HPC/AI Devices

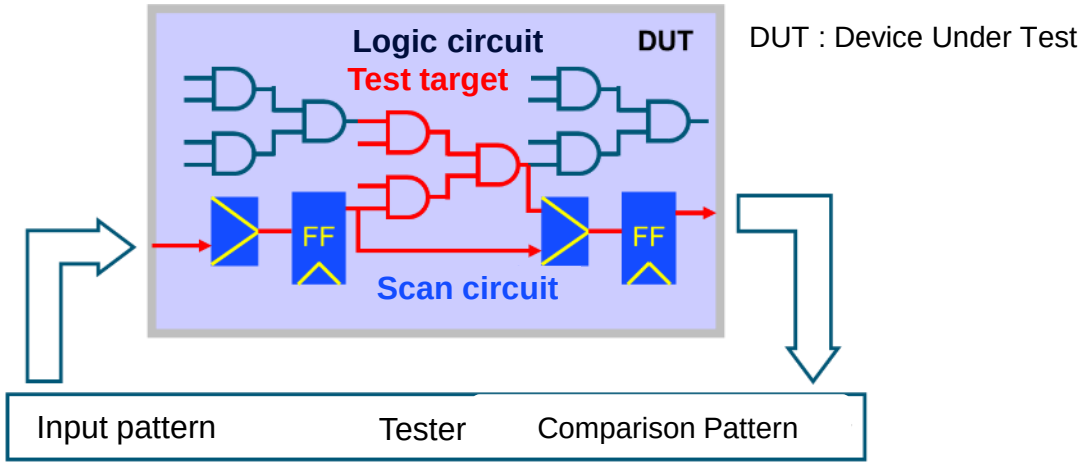
HPC/AI Devices Logic Testing



Scan test

- Typical item of DFT (Design for Testability)
- Main test item for SoC devices from the 2000s to the present

- Scan circuits are inserted in the device to arbitrarily set conditions of the sites to be measured
- Generate test patterns based on assumed failure models and locations
- High efficiency /high test coverage (95 to 99.5%)

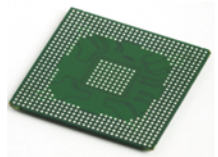


DUT : Device Under Test

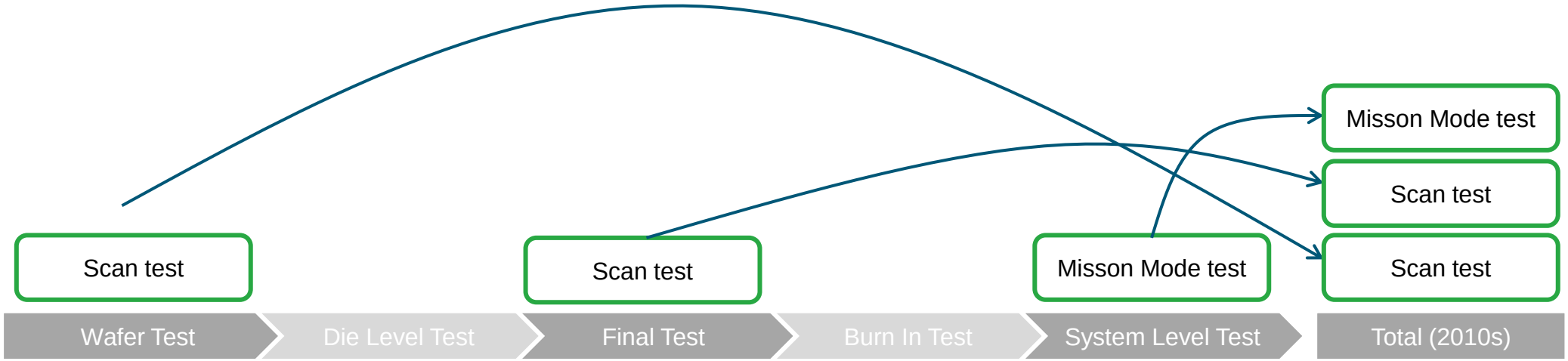
Increasing transistor count causing lengthening of “test patterns” = Lengthening of test time

Test in the 2010s: Screening of Defective Devices

- ✓ Wafer Test：test each die individually,　Final test：test each packaged die individually
- ✓ Test Volume：Wafer Test ≒ Final Test（Package Test）
- ✓ Test items optimized for front-end and back-end processes, respectively
- ✓ System level test is added depending on the application



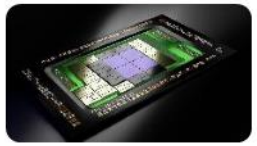
Note: The height of the boxes in the image does not correspond to the test times for each test



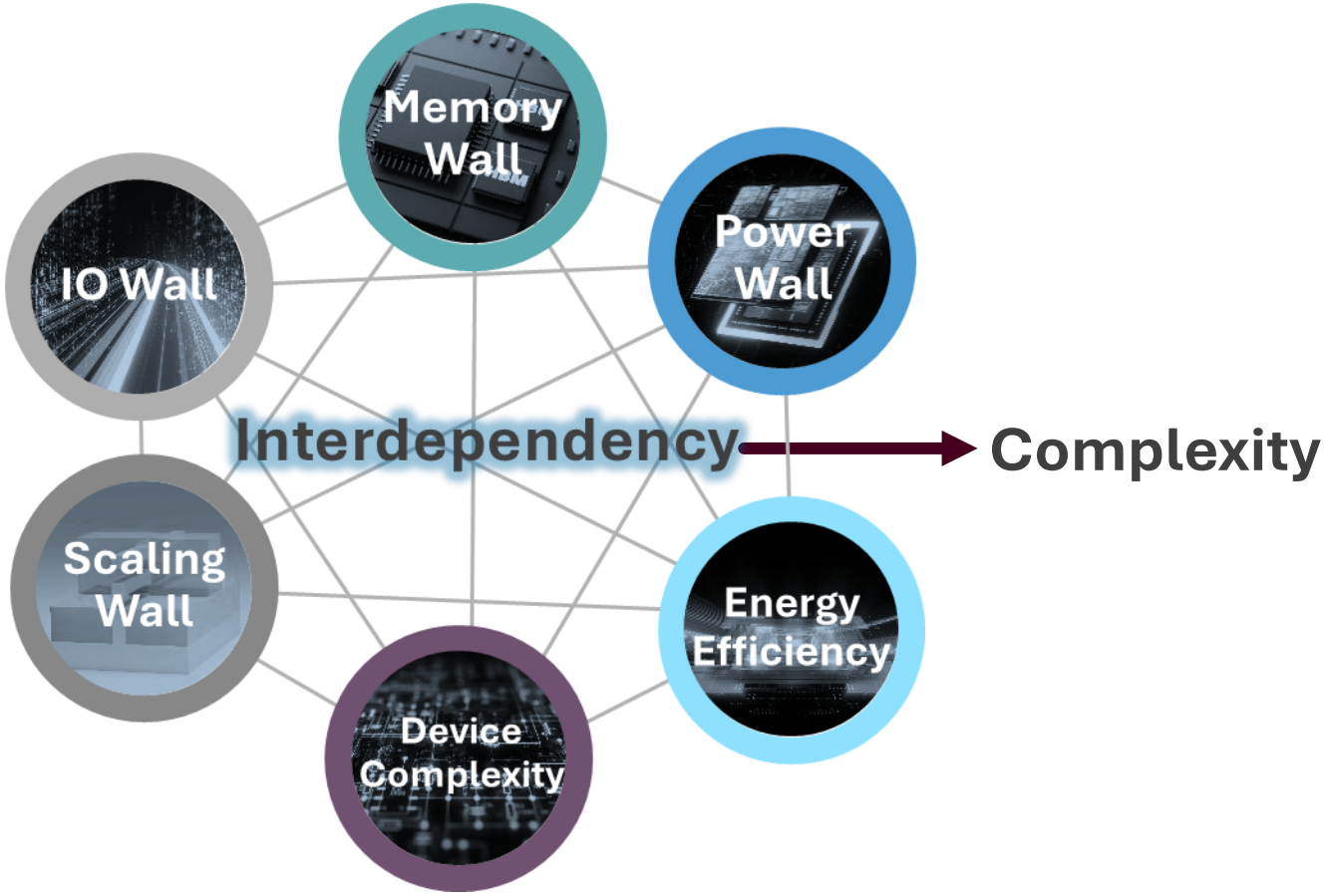
Test in the 2020s: More Complex, Longer Test Time

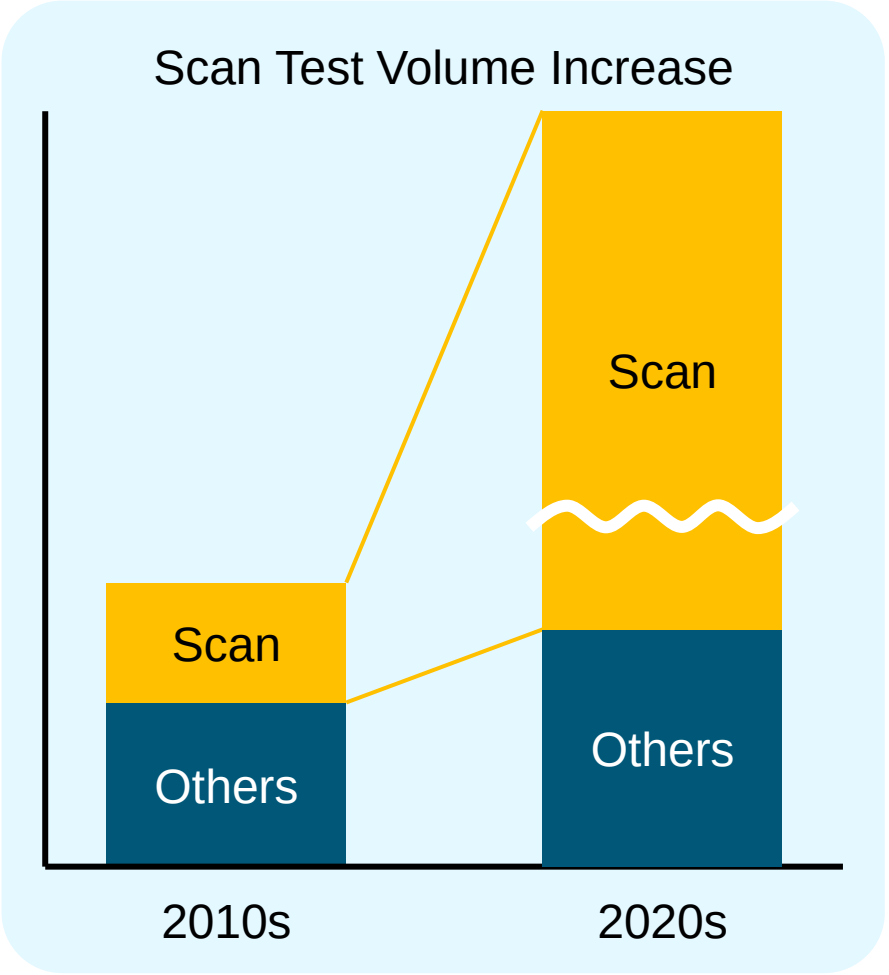
Note1: The height of the boxes in the image does not correspond to the test times for each test.
Note2: Items in the red boxes are factors driving demand growth in the 2020s.

- ✓ An increase in scan test volume due to increased number of transistors and new failure models
- ✓ Additional test insertions for die-specific characteristic measurement and an increase in test contents in final test due to multi-die assembly
- ✓ Increased efforts to further ensure high quality, including multi-temperature test, burn-in, and system level test

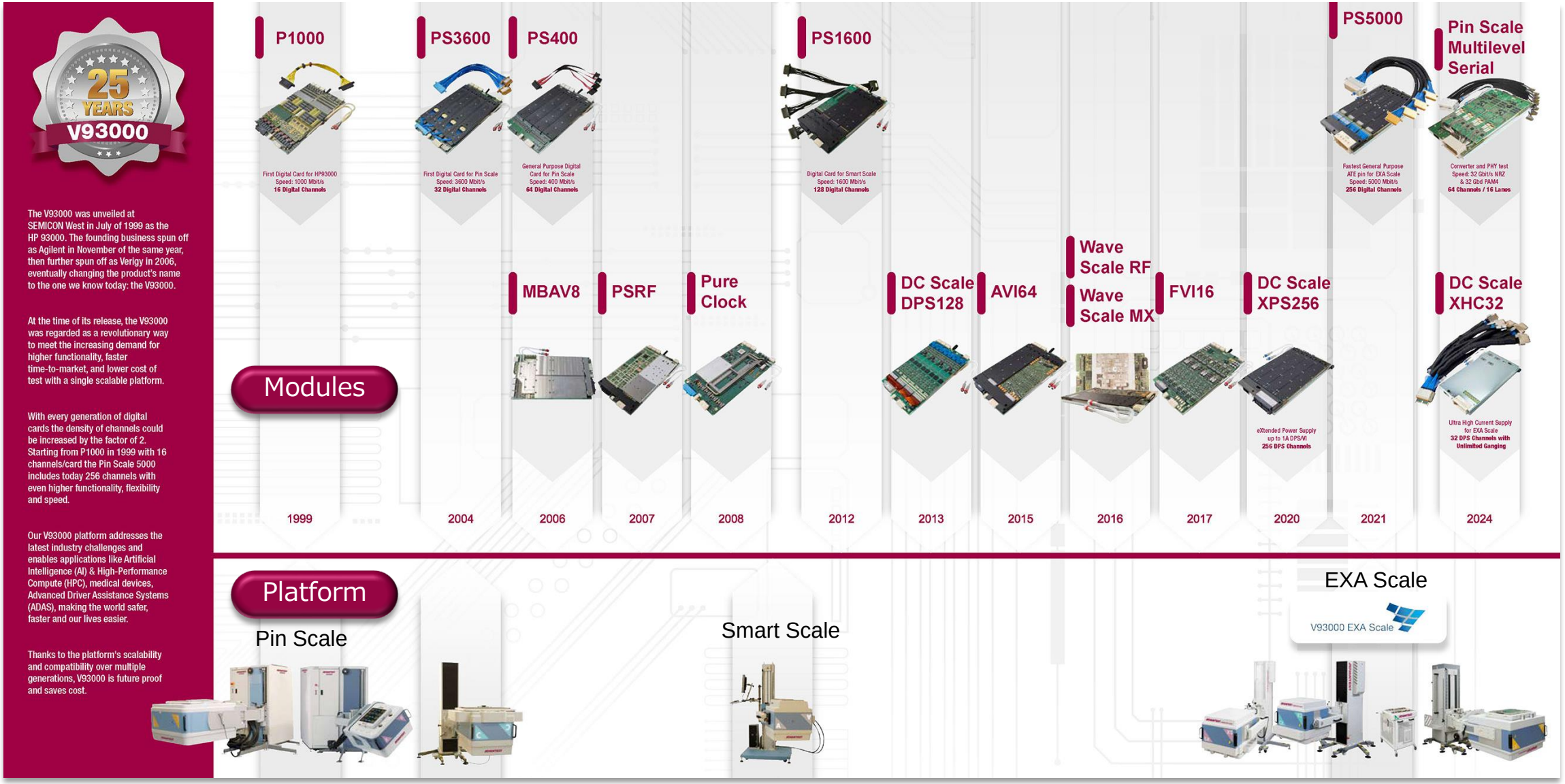


Test Demand Driven by Accelerating “Complexity”





V93000 - The Scalable SoC Test Platform



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