Advantest Corporation
FAQs Summary post Briefing on Mid-/Long-Term Management Policy

<div align="right">Date of Publication: July 23, 2024</div>

＜Market Assumptions＞

Q1: What businesses are specifically included in "Semiconductor test (ATE) and existing domain" and "Extension" which constitute the "Core market" as illustrated on p.29 of the Briefing material? Please provide a definition and breakdown.

A1: "Semiconductor test (ATE) and existing domain" includes test handlers, Mask-SEM which is part of nanotechnology products, and maintenance services, all of which are existing domain products, in addition to the ATE market for which we have been providing the TAM estimate. "Extension" includes system level test, high end test sockets, test interface boards, and cloud data infrastructure. We do not disclose the breakdown of each of these product areas because the data compiled comes from third-party research vendor companies, with the exception of semiconductor testers and maintenance services.

Q2: On p.30 of the Briefing material, the semiconductor test (ATE) market size is forecast to be 5.9 billion USD on average over the three years between CY2024-26. Please provide the market size estimate for each CY and a breakdown of the market size estimate into SoC testers and memory testers.

A2: We consider it premature to disclose individual annual market size estimates and a breakdown of the ATE market at this time. In line with our usual disclosure practice, we plan to unveil our market size estimates for CY2025 and 2026 in January of the respective year.

Q3: Third Mid-Term Management Plan (MTP3) assumes Advantest's market share in the ATE market will be 58% or more, up from 54% in the MTP2, as shown on p.30 of the Briefing material. Under what circumstances can this increase in market share be expected?

A3: The market share assumption is based on increased sales to existing and new customers in the growth area of AI/HPC. You may feel our assumption of 58% or more is conservative. However, if one assumes a market recovery in the MTP3 period not only in the growth area of advanced processes but also in mature processes, the mix between advanced and mature processes will also be a factor in the increase in our market share.

＜Cost/Profit Target Model＞

Q4:   Please provide the upper and lower ends of the ranges of the MTP3 management metrics
      on p.31 and the assumptions made for each.

A4:   In anticipating a growth cycle starting in FY2024, we believe that there will be a certain
      degree of swing in demand. Based on this assumption, the lower end was set as the
      minimum three-year average level to be secured even in an environment where sales fall
      more than expected, as in FY2023. Conversely, the upper limit end set as a management
      metric in a better-than-expected environment.

Q5:   The target model on p.32 shows a gross margin of 53%; what is the assumption for the
      recovery of the gross margin from FY2025 onwards?

A5:   The largest contribution to improved profitability comes from an increase in the sales mix
      of high-end SoC semiconductors. This is followed by the effect of measures to improve
      profitability for HBM is factored in. The specific measures for HBM include the following
      two steps: (1) increasing the average selling price by upgrading test solutions for existing
      products and (2) selling testers with high added value by developing new testers that
      support technological evolution, such as the shift to HBM4.

Q6:   In the Briefing, there was an emphasis on improving operations; what was the backdrop
      for such an emphasis?

A6:   In FY2021 and FY2022, fixed costs increased as the Company increased its workforce
      amidst business expansion; in MTP3, even as business expands, the Company aims to
      increase its operating margin by managing SG&A expenses appropriately. In an era when
      the use of AI in operations is taking shape, we will seek to increase business value and
      profitability through initiatives such as the promotion of DX.

＜Strategy＞

Q7:   What is meant by 'EDA linkage' as described on p.19 and 20 of the Briefing material?

A7:   'EDA linkage' refers to the mutual compatibility between the EDA tools used at the
      design stage and the test data on the tester level. By creating a bridge tool that can
      complement such mutual language differences, we want to contribute to the reduction of
      defects at the customer's design stage. While we pursued these initiatives during the MTP2
      period, we believe that the MTP3 period is a time to further deepen collaboration with our
      partner EDA vendors.

Note

The document has been revised and edited by Advantest for ease of understanding based on questions received following the Briefing on Mid-/Long-Term Management Policy.

This document contains "forward-looking statements" that are based on Advantest's expectations, estimates and projections as of the timing of the MTP3 announcement. These statements include, among other things, the discussion of Advantest's business strategy, outlook and expectations as to market and business developments, production and capacity plans. Generally, these forward-looking statements can be identified by the use of forward-looking terminology such as "anticipate," "believe," "estimate," "expect," "intend," "project," "should" and similar expressions. Forward-looking statements are subject to known and unknown risks, uncertainties and other factors that may cause Advantest's actual results, levels of activity, performance or achievements to be materially different from those expressed or implied by such forward-looking statements.