Advantest Corporation
FY2025 Q1 (Three months ended June 30, 2025) Financial Briefing
Q&A Summary
July 29, 2025

CY2025 tester market size estimate

Q1: You raised your CY2025 SoC tester TAM estimate, increasing the midpoint by more than 30% from 4.5 billion dollars to 6 billion dollars. How much of that is premised on higher chip volumes and how much is premised on increased test times?

A1: Before discussing test content or unit volume, permit us to provide some context. When we released our TAM forecast in January and April, the business environment was highly uncertain due to factors such as tariff discussions. Many companies pulled their full-year guidance, but we wanted to put our best estimate forward even though there was great uncertainty.
Therefore, some of the approximately 30% increase stems directly from the caution that we had chosen to exercise in our January and April forecasts because of the uncertainties at play at those points in time. In terms of test content versus unit volume, we would lean more toward unit volume as there were adjustments in wafer starts and advanced packaging capacity that created unanticipated demand that we were able to respond to in CY2025 1H.

Q2: You raised your forecast for your own SoC tester sales by only around 20%, less than the increase you made to your estimate for the SoC tester TAM. What explains that disconnect?

A2: One issue is that our sales numbers are on a fiscal-year basis, whereas our TAM numbers are on a calendar-year basis, which leads to some discrepancy. In our Third Mid-Term Plan, our KPI for overall market share is greater than 58%. On SoC testers, we continue to be above that metric, and we are also above that for memory testers. The calendar versus fiscal year creates some confusion, as do exchange rate fluctuations since we have the TAM in US dollars and our sales in Japanese yen.

Market share/competitive environment

Q3: Is it fair to assume that while you have increased your forecasts for the SoC tester TAM and your sales, you do not anticipate any major changes in your market share? Could you also speak to the competitive environment in your SoC tester business? What does the competition with your US peer look like in testers for GPUs and custom ASICs?

A3: On a general level, our share in SoC testers has gone up. In memory testers, our share remains relatively steady.
We are positioned very well right now and should continue to hold our current market position. It is very difficult for customers to switch test platforms in the middle of ramps. For the foreseeable future, we believe we have a very strong market and competitive position, both in GPUs and custom ASICs.

Q1 FY2025 Results

Q4: Why did your FY2025 Q1 earnings beat your expectations? Did tariff policies play a part, for example? Alternatively, did something drive a temporary demand surge?

A4: On the sales side, there were many pull-ins. We had not originally expected quarterly sales to be so substantial and had thought demand would be more spread out. However, we saw a significant volume of pull-ins, and underlying demand was also higher than we had originally expected.
On the profitability side, the stars aligned perfectly for us in Q1. There was a really good product mix, and economies of scale and efficiencies. In addition, we did not have any one-time write-downs. That all led to this great result in Q1.

Q5: I would like to ask about your earnings outlook for FY2025 Q2 and beyond. How sustainable do you believe the strong performance you saw in Q1 was? Also, do you not think 2H earnings could exceed your forecasts?

A5: Some of the factors that drove our strong Q1 results are sustainable and some are not. On the sustainable side, product mix may not be quite as good, but it should still be very rich with SoC versus memory. We also expect some of the efficiencies that we are driving to continue. However, the Q1 performance was very special with everything aligning perfectly. It would be irresponsible to suggest that we can have a quarter this big in the future.
As we look into FY2025 Q3 and Q4, we are likely to see the aforementioned pull-ins result in lower sales. There are also numerous device transitions underway. Some of the big AI accelerators on both merchant GPUs and custom ASICs are coming up, and there are HBM transitions on the memory side. As such, we are seeing substantial investment undertaken to bring up those new types of devices that will show up later, more likely in FY2026.

Q6: Could you share the split between GPUs and custom ASICs in your FY2025 Q1 SoC tester sales?

A6: We are not able to provide that split because it involves customer-specific information that we avoid disclosing. Currently, it is still largely traditional GPU-based. We see custom ASIC growing now and expect it to represent a larger portion in 2026.

FY2025 full year outlook

Q7: You say that you anticipate a correction in FY2025 2H, but what are you expecting the quarterly earnings trend to look like in FY2025 Q2 and thereafter?

A7: Q1 was a banner quarter. We expect Q3 to be the lowest point of the year, with sales improving in Q4 and that growth likely continuing into FY2026.

Outlook for FY2026 and beyond

Q8: At your April results briefing, you expressed optimism about CY2026. What is your current outlook for FY2026? Can you expect to see sales growth versus FY2025?

A8: We are very optimistic about FY2026, when we expect to see a reacceleration. Additional wafer capacity and advanced packaging being added will drive additional unit volume and test capacity needs. Hyperscaler capex growth is remaining intact, which is also encouraging.

Additional test content will be required as devices continue to gain complexity. We are also hopeful that the consumer and automotive segments will return to growth. There is therefore no reason at present to believe that FY2026 will be a down year. We will provide more details as we get further into the year and have more visibility.

Q9: You have described a very constructive outlook for CY2026. Given industry trends, what is your view on CY2027?

A9: As we look beyond CY2026 to CY2027, we view wafer starts and the advanced packaging capacity being put in place by our customers as signals. Hyperscaler capital budgets are another reference point. In both cases, there has been enough public discussion around continuation of current trends. If those trends continue, there is optimism that this growth cycle will continue beyond CY2026 into CY2027.

However, we know from experience that cycles can change quickly, so our approach to managing the company does not assume that that is going to be the case.

Production capacity expansion

Q10: You say that you plan to expand your production capacity by more than 70% compared to FY2024. What is the timeline for that target? Also, what is the baseline for the capacity expansion for SoC testers?

A10: We are able with our current capacity to meet all the current needs of our customers. We have roughly tripled capacity in the last several years. For this next step function in capacity additions, we are targeting the end of CY2026 to add capacity for both our SoC tester platform and memory tester platforms.
The 60-70% expansion on the SoC side is going to be based on our 2025 levels. We are not just building capacity to meet the next wave of demand. We are putting additional capacity in place to handle some of the volatility that we have seen from unanticipated demand. We have learned that it is very difficult for customers to forecast spikes from AI-related waves. For us to respond quickly to such demand, we have to build additional buffer levels of capacity to meet those spikes. From a baseline level, without quoting an exact number, we can ship more than 3,000 of our 93k systems per year at present.

Q11: Is the capacity that you are adding permanent or temporary?

A11: Because we have a long-term belief in the industry getting to one trillion dollars in semiconductor revenue, we know that we are going to have to add this type of capacity in a permanent fashion. As such, this would not be temporary capacity. Even longer term, we probably will have to expand further, and we have already initiated some of those plans.

Die level test

Q12: My understanding is that prior to the growth in AI demand, wafer sorts and final test accounted for roughly equal percentages of tester demand. How do you view that split now that chiplet architecture is becoming more commonplace and chiplet volumes are growing? Do you expect growth in wafer tester demand to drive continued growth in Q4 and beyond? And, are you seeing changes in die-level test demand?

A12: The importance of wafer sort is growing as chiplet strategies make packages increasingly expensive, driving up the value of known good dies(KGDs*). We expect this business to grow faster than final test, with die-level-testing representing exciting new opportunities. This emphasis on known good die testing at the silicon level will require new solutions, particularly thermal control capabilities at the die or partial assembly level, which is not possible with monolithic wafers. These evolving test flows at the wafer and die level will likely create additional test insertion points, all of which we see as significant upside opportunities.

*Known good die (KGD): A bare die verified as meeting quality standards

Memory tester business

Q13: Do you expect device bit growth or generational transitions in HBM will drive HBM-related memory tester demand going forward?

A13: We are optimistic about our memory tester business, and several factors contribute to this outlook. HBM serves as a key growth driver, with customer transitions to HBM4 and HBM4E expected to drive increased tester demand, along with higher stack configurations. Beyond HBM growth, we maintain a very favorable product mix and market dominance, particularly in DRAM, which reinforces our confidence in the memory tester business. We think the growth should continue as AI demand persists and data center builds continue. That will drive more and more product volumes, and for memory products as well. There should be a good growth opportunity for us.

Adjacent markets

Q14: I would like to ask about growth in adjacent markets, including services. In which of such fields do you expect to see growth?

A14: Several areas drive our growth expectations. System-level test (SLT) represents significant opportunities as nodes shrink and testing demand increases. We continue investing heavily in this area and expect substantial business growth.

Our device interface (DI) business shows strong potential as we have invested strategically and more customers demand turnkey applications. Engineering services and warranty support benefit from organic growth driven by an increased installed base, as our results demonstrate.

Additionally, customers increasingly expect expanded capabilities, creating opportunities in new service areas we have yet to address. While these initiatives remain under development, we anticipate meaningful contributions to our business results.

Changes in reporting segments

Q15: Why did you move your test handlers and system-level test into the Test System Business?

A15: Our previous Mechatronics Systems segment was somewhat outdated given our current business environment. We simplified it into two segments—“Test System Business” and “Services & Others“—which better aligns with industry standards.

Note

This document is prepared for those who were unable to attend the financial briefing and is intended only for reference purposes. The original content has been revised and edited by Advantest for ease of understanding.

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