Advantest IR Technical Briefing

Demand Changes and Our Solutions in System Level Test (SLT)

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NOTE

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Today’s Agenda

✓ Changes in Business Environment of System Level Test (SLT)

✓ Opportunities in the “New” SLT Market

✓ Summary
Changes in Business Environment of System Level Test (SLT)
Our Grand Design (FY2018 - FY2027)

Background: Change in the Tester Market

**PAST**
Mainframes → PCs
→ Smartphones

- Smaller, Cheaper
- Greater Tester Efficiency

**FUTURE**
Data Takes the Spotlight
Semiconductors as Infrastructure

- Greater Semiconductor Functionality, Complexity, Capacity
- High Reliability

More Test Items & Longer Test Times × Greater Difficulty of Failure Detection
= Test to be Reinforced to Guarantee Reliability

**Test will Become More Important and More of them will be Needed**
Adding Customer Value in an Evolving Semiconductor Value Chain

Grand Design: Our Vision

CLOUD, AI, & DATA ANALYTICS

Our Existing Business Domain

IC System Level

Design / Evaluation Processes

Production processes

Wafer test / Final test

SEMICONDUCTOR VALUE CHAIN

IC System Level

System Level

Product / System Level Test Process

2019

2020

essai
Changes in the Test Flow for High-end SoCs

Advanced technology is driving changes in test requirements and the test flow.

PAST

Wafer Sort Test → Package Test → System Level Test

SLT was limited to few applications only

NOW

Wafer Sort Test → Package Test → System Level Test

Chip test enhancement driven by adoption of multiple test process and longer test time, more complex IP and roll out of advanced packages

SLT is being adopted for “Mission Critical” applications with fully integrated manner

Advanced technology is driving changes in test requirements and the test flow.
Market Mega Trends Driving System Level Test

- **Memory & Storage**
  - Cloud storage
  - New protocols

- **Computing**
  - AI computing
  - Cloud/Edge computing

- **Mobile**
  - 7nm and lower

- **Automotive**
  - ADAS
  - Infotainment

- **Thermal Management**
- **Heterogeneous System Integration**
- **High Speed Protocol Interfaces**
- **High Unit Volumes**
- **High Performance**
- **Advanced Packaging**

Those Mission Critical Applications are our SLT Market
Voice of Customers

“High volume production System Level Testing”

“World class DPPM needed”

“Applications with thermal control to guarantee quality”

“Multi-IP testing under system load with thermal control”

“Complex power management features during system operation”

“High-speed interface testing”
Opportunities in the “New” SLT Market
What is Conventional System Level Test (SLT)?

Example: GPU for Server
- IC (DUT) is temporarily placed in a socket on the Customer Bench Application Board
- PC with software and power supplies are connected to Application board
- Tests similar to end user scenario are run with real software

Typical tests:
- Boot – 90% of failures from device maker are boot failures
- Play a video, run a graphics app, run a computing benchmark, simultaneously

System level test ensures devices are tested similar to end user functionality. SLT cannot and does not replace ATE testing.
What is Conventional System Level Test (SLT)?

Conventional System Level Test Primarily Sampling Based
Low Site Count Architecture Designed for “Sampling” and Low Volumes, Fixed Cost / Site
Customer Challenges lead to System Level Test

**NODE SHRINKAGE**
- Increasing Transistor Count
- Higher quality assurance
  - Even 99.5% test coverage leaves test escapes

**PACKAGING**
- Complex 2.5D and 3D
- Technology Complex packaging limits ATE access

**SYSTEM**
- Integration and User Scenarios
- Higher quality assurance
  - Correct operation requires software interaction

**PROCESS**
- Control PVT/DVFS Explosions
- Higher quality assurance
  - while managing and balancing test costs

**YIELD**
- Reduce Overkill
- Increase Yield
  - Guardbanding limits operating range while the part works well in the system

All technological evolution calls for enhanced quality assurance
The Path to Massively Parallel System Level Test

Advantest Industrial Automation of System Level Test

System Level Test goes mainstream – it’s here and Advantest makes it affordable at production scale

Advantest provides fully integrated and massively parallel system level test solutions
The only truly global supplier delivering expected customer value
Key Advantages of Advantest Test Solutions

- Global, Reliable, Experienced
- Automation for High Volume Manufacturing
- Active Thermal Control (ATC)
- Customer Relations
- Integrated Communication & Power Delivery
Essai’s Products Strengthen Advantest’s value

Next generation Peltier enables higher Yields
• Enables large form factors
• Higher heat density management
• Improved temperature control across wider ranges

Modularized temperature control unit (TCU)
• DUT specific change kit
• Smarter serviceability design enabling higher uptime

Bringing new innovative probe technologies to market:
• Patented full stack coaxial shielding technology
• Revolutionary Titan BGA probes with life-time CRES consistency

Wide array of socketing technologies across:
• Package types
• Form factors
• Grid arrays & pitches
Summary
Key Drivers of Market Growth

- Semiconductors are becoming more sophisticated and more complex, with larger capacity, which are driven by digital transformation.
- All of these factors lead customer demand to ensure higher quality assurance by stringent testing.
- Expect more customer interest for the combination of DFT and functional testing by ATE, real case performance testing by SLT, to maximize test coverage and improve quality.

Along with greater “Mission Critical“ applications and semiconductor complexity, higher demand for quality assurance will continuously expand SLT market.
Uniquely Positioned to Deliver Increased Value Across the Chain

• As Data moves to the forefront, time-to-insight of the semiconductor test data grows increasingly more important.

• Globally recognized as a leading global ATE supplier, Advantest continually delivers world class quality and reliability within a competitive cost envelope extended into SLT further improving customer value.

• Advantest is uniquely positioned with fully integrated ATE and SLT solutions across the entire semiconductor test chain to link the important components.

Our Belief

A superior integrated technology position which fully integrates Advantest’s tester, handler, thermal, socket, and data technologies is necessary to deliver upon and exceed customer value and expectations.
Advantest Uniquely Positioned Across Entire Test Life Cycle

In this presentation, DFT is referring structural test for ICs which include design for test architecture.

**ATE ensures design specs and is fabricated per the design**

**Combination of DFT, functional and SLT leads to maximum test coverage and best Time to Value**

**SLT ensures system performance of the final system**