Advantest Corporation
IR Technical Briefing
Q&A Summary

November 29, 2023

Q: What is the scale of tester sales for HBM (High Bandwidth Memory) and its future prospects, as well as market share outlook? Also, what is the difference in test time for wafer tests between HBM and conventional DRAM?

A: The full-year sales forecast for memory testers disclosed in FY2023 2Q Financial Briefing is 76 billion yen, of which approximately 90% is expected to be for DRAM. Of that, we estimate that about 60% is for wafer testing, with HBM accounting for more than half. As for the scale of sales for the next fiscal year, we are currently examining the business opportunities, but we are considering to gradually increase our tester production capacity by 1.5 to 2 times on a unit basis from the current level.
As far as we are aware, in the current initial ramp up phase, most of the tester demand for HBM has been secured by us, given the high level of trust backed by our wafer tester installed base and our track record in testing. However, memory semiconductor customers have a dual vendor policy, and the possibility of competitors entering the market in the future cannot be ruled out. We intend to take advantage of our tester track record and installed base which we have accumulated during this initial ramp up phrase and play them to our strength in our future business negotiations as well.

The test time for HBM is longer than for standard DDR5 testing due to the additional test process after stacking wafers into 8 or 12 stacks. Test time is customers' confidential information. Since test specifications and the number of test process vary from customer to customer, it is difficult to generalize the length of test time quantitatively. However, our impression is that test times are longer for HBM due to the increase in memory density and additional test process due to stacking as well as higher quality assurance requirement.

Q: I would like to ask about HBM testing process. Is it correct to assume that once DRAM wafers are tested and stacked on a logic wafer, it will be followed by a stacked wafer test again? For a stacked wafer test, what kind of testing is conducted and which testers are used? Also, my understanding is that high-speed testing after packaging is a high value-added method of DRAM testing. Therefore, what impact does the company expect in

terms of profitability, given lower demand for packaging test and higher demand for wafer test?

A: As shown in the left figure on page 16 of the presentation material, HBM consist of DRAMs which have been tested in wafer form and are stacked on a logic wafer which has also been tested in wafer form. After stacking, HBM will undergo testing in wafer form. For an illustrative purpose, this diagrams shows three test processes after stacking, but there may be cases in which four or more processes depending on the customer, with different temperature environments and test parameters. Under those circumstances, customers are attempting to conduct complex tests including I/F (interface) speed test which is a process to test functioning of DRAM at high-speed.

The same memory tester is used for both the initial DRAM wafer test and after-stacking HBM stacked wafer test, but the test conditions requirement are different. After-stacking test requires a higher level of test performance in terms of test speed and function testing. We expect that tester configurations for wafer testing will need upgrades to perform more complex, value-added tests with higher functionality, equivalent to conventional after-packaging I/F speed tests, which means that the added value of the testers will also increase. In addition, since the number of memory semiconductors that can be tested simultaneously is limited for such complex tests, the number of testers required is expected to be larger for post-stacking HBM test compared to standard DRAM wafer tests.

Q: What is the future growth rate forecast for the memory tester market for HBM? A chart on page 15 of the presentation material shows that CAGR of HBM itself is 49% (in bit base) from 2023 to 2028. Does the Company expect similar growth rate for tester demand?

A: In 2024 and 2025, we expect the memory tester market for HBM to grow at approximately the same rate as HBM, given it is still in the ramp up phase. However, from 2026 onward, we believe that as HBM quality improves on the customer side, customers will also try to pursue testing efficiency. When it comes to such a phase, it is necessary to gather information and assess the potential growth rate of the tester market.

Q: I would like to ask about the prospects for testing after dicing wafers for HBM. I don't think that testing after dicing is currently being conducted, but I have heard that post-dicing failures are being viewed as a problem. As quality assurance requirements for HBM increase, will testing be required not only at the wafer level but also post-dicing?

If this were to happen, it would likely be a considerable plus in terms of profits, as it would boost sales of highly profitable package testing in your memory tester business.

A: Memory semiconductor manufacturers, who are our customers, are also discussing the quality of semiconductors before and after dicing (into chips). Currently, semiconductors are shipped after testing in wafer form, but we are discussing with customers potential test methods including handling technologies and discussing whether it is possible to test semiconductors in post-dicing form. Accordingly, we are working on development of the elemental technologies that may be necessary.

If we can establish a test methodology for post-dicing tests using our memory testers and test handlers, we will be able to perform I/F speed testing in a conventional package test environment.

Q: What is the future outlook for memory tester profitability as tester sales for HBM are growing?

A: As memory testers become more advanced alongside advancement of memory semiconductors, testers offer greater technological value-added and enjoy improved profitability. For HBM testing, performance improvement required is one or two levels higher than conventional wafer test. Accordingly, we expect that we will be providing product upgrade solutions, which should result in profitability improvement compared to the existing wafer test business.

Q: As the generational shift in HBM continues, does the Company plan to launch new products?

A: Our understanding is that our current products can cover the initial generation of HBM4. However, the specifications for HBM4 have not yet been finalized, and testing methods have not yet been finalized. Therefore, we may need to add functions to our existing products, but we do not believe that we will need technologies that we have never experienced before.

On the other hand, we are constantly developing technologies to improve customer value and competitiveness. We have a product development schedule in place to release more competitive products that are compatible with next-generation memory in a timely manner, and we will announce such products in due course.

Note

This document is prepared for those who were unable to attend the IR Technical Briefing and is intended only for reference purposes. The original content has been revised and edited by Advantest for ease of understanding.

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