ADVANTEST®

ADVANTEST CORPORATION

INSTRUCTION MANUAL

TR4720-540

Personality Kit

For Z 80

MANUAL NUMBER 0820 EB 110

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Printed in Japan

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CHAPTER 1
GENERAL

1.1 INTRODUCTION

The TR4720-540 Personality Kit, installed in the TR4720 Logic Analyzer, can be used to perform total debugging of various systems incorporating Z80 microprocessors. The principal features of the TR4720-540 are as follows:

1) Since this personality kit is peculiar to the Z80 microprocessor, the setup operation for measurement is easy and data can be fetched smoothly.
2) Since mnemonics peculiar to the pertinent microprocessor can be displayed with the disassembling function, obtained data can be analyzed very easily.
3) The TR4720 trigger function is improved with the data bus qualifier.
4) Since the test pattern generator generates test patterns similar to microprocessor signals, various tests, from the CPU probe test to the TR4720 basic measurement function test, can be performed.
5) Since high-speed hardware is used to fetch data, the TR4720-540 can be used to cope with a high-speed microprocessor in the future.

NOTE

This Instruction Manual explains the functions peculiar to a specific microprocessor. Refer to the TR4720 Logic Analyzer Instruction Manual for functions common to various object microprocessors.

1.2 PERSONALITY KIT CONFIGURATION

Personality Board 1

Microprocessor Probe (connects the TR4720 to the system under test) 1

Probe connectors

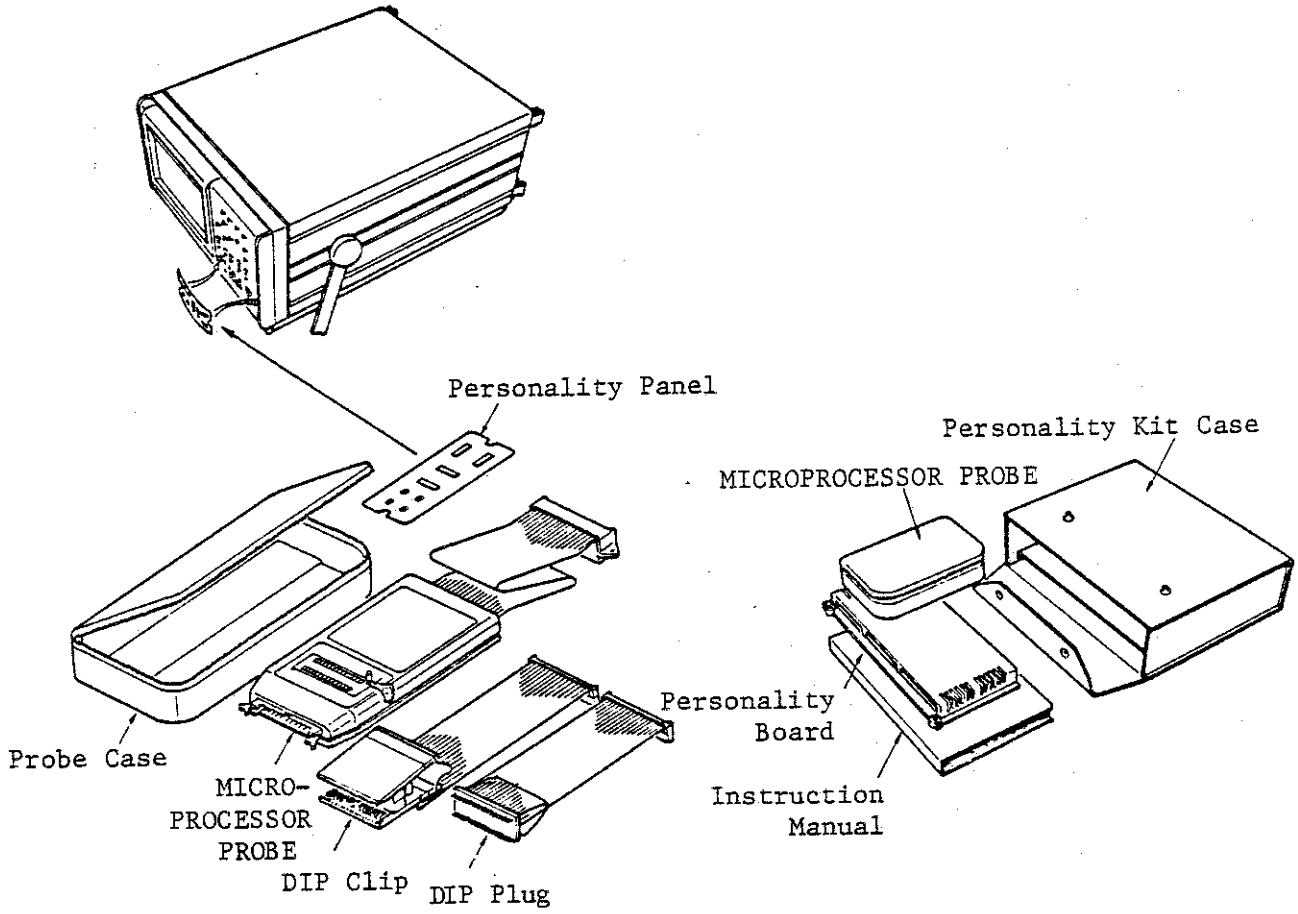
- 40-pin DIP clip connector 1
- 40-pin DIP plug connector 1

Personality Panel (mounted on the TR4720 front panel) 1

Microprocessor Probe Case 1

Personality Kit Case 1

Instruction Manual 1



1.3 SPECIFICATIONS

Applicable Microprocessors: ZILOG Z80, Z80A, Z80B, and equivalent

Clock Frequency: Varies with system to be measured (8 MHz max.)

Input Current: -200 μA max. (low level)
+20 μA max. (high level)

Qualifier: ⓐ OP or OFF
ⓑ READ, WRITE, or OFF
ⓒ MEMORY, IO, or OFF
(ⓑ and ⓒ are ANDed, then the result is ORed with ⓐ.)

CPU status display:

BUSAK: Goes on when the microprocessor $\overline{\text{BUSAK}}$ signal is low.

HALT: Goes on when the microprocessor $\overline{\text{HALT}}$ signal is low.

WAIT: Goes on when the microprocessor $\overline{\text{WAIT}}$ signal is low.

WAIT BY L.A.: Goes on when the microprocessor WAIT signal is issued from TR4720 to the microprocessor.

TRACE THEN WAIT: Operates when the microprocessor is connected to the probe in TRACE mode. The microprocessor WAIT signal goes low after a trace execution.

CHAPTER 2
SETUP

2.1 CHANGING PERSONALITY KIT

If the personality kit already installed in the TR4720 is not applicable to the microprocessor to be measured, it must be changed. This section explains how to change the personality board, personality panel, and microprocessor probe.

2.1.1 Changing Personality Board

1) Set the POWER switch to OFF.
2) Remove the four Phillips-head screws (3 mm) on the TR4720 top cover, then remove the top cover.
3) Viewed from the front panel side, the personality board is located at the right end. Remove the three connectors on top of the personality board.
4) Disconnect the board by pulling the finger grips on both sides of the board. (See Fig. 1)
5) Insert the personality board to be used along the board guideways on both sides with the nameplate (see Photo 1) facing outward.
6) Connect the three connectors on top of the personality board.
7) Mount the TR4720 top cover, fixing it with four screws.
8) Set the POWER switch to ON, then check that the object microprocessor name of the inserted personality board is displayed on the CRT display approximately 30 seconds later. (See Photo 3)
9) Store the removed personality board in the pertinent personality kit case.

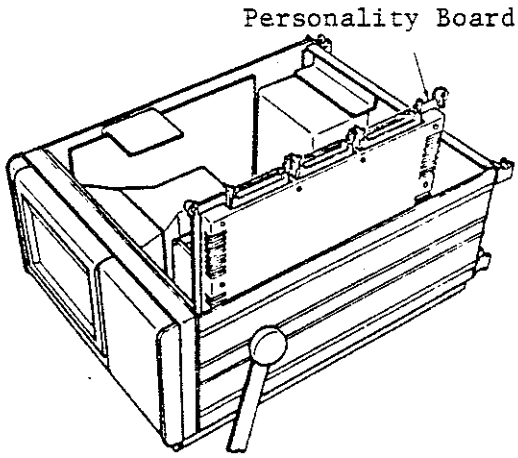


Fig. 1 Personality board change

2.1.2 Changing Personality Panel

1) The personality panel is on the lower-right side of the front panel. Set the TRIGGER QUALIFIER switches to READ and MEM. Since the personality panel is made of plastic, it can be removed by bending it from the CPU STATUS LED side.
2) Mount the personality panel to be used by fitting its notches to the decorative screws. (See Fig. 3) Set all TRIGGER QUALIFIER switches to OFF.
3) Store the removed personality panel in the pertinent Microprocessor Probe case.

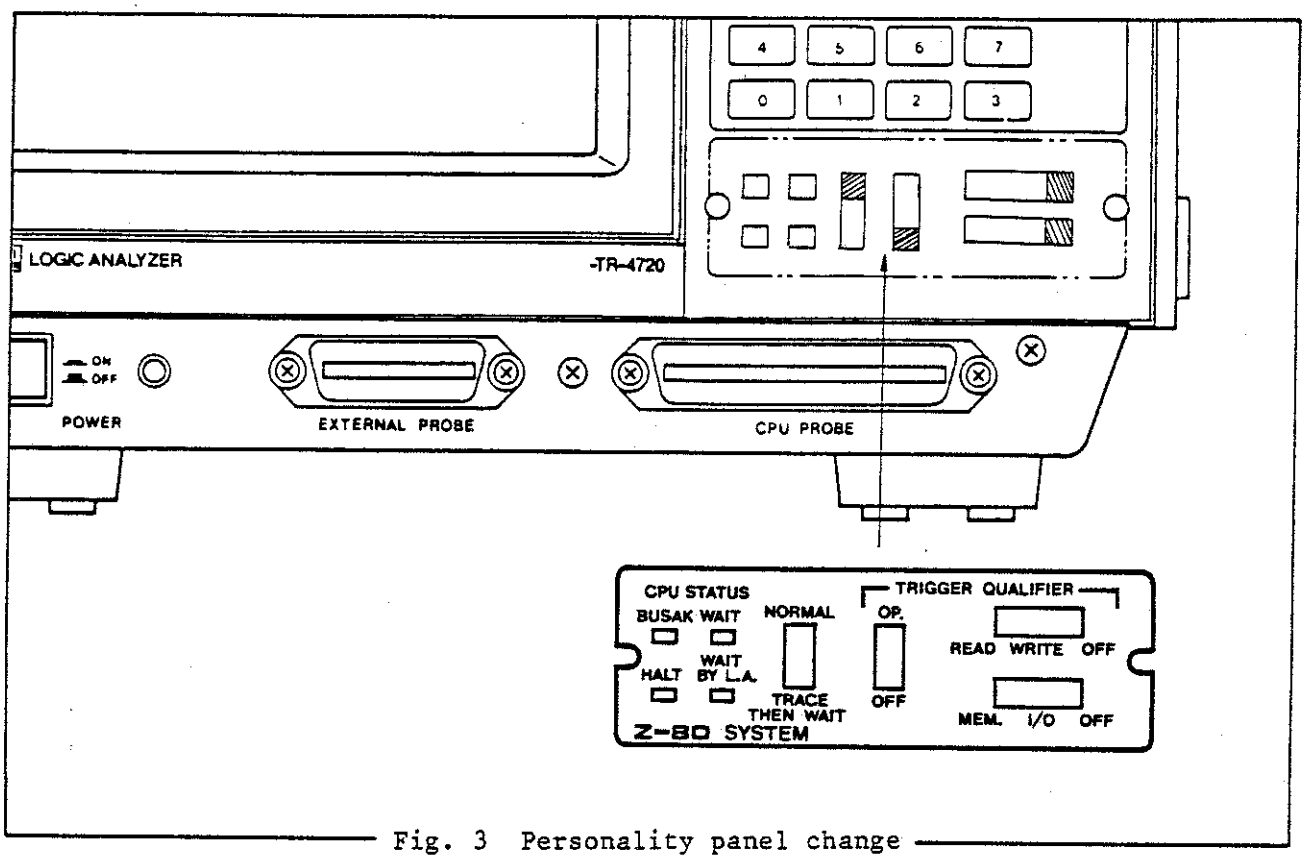


Fig. 3 Personality panel change

2.1.3 Changing Microprocessor Probe

1) Connect the appropriate Microprocessor Probe (see Photo 2) to the CPU PROBE connector at the bottom of the front panel.

2) Store the removed Microprocessor probe in the pertinent Micro Processor Probe case.

2.2 MICROPROCESSOR CONNECTION

There are two types of connectors for connecting the Microprocessor Probe to the microprocessor of the system under test (SUT). (See Fig. 4)

1) 40-pin DIP Clip Connector

Clip the SUT microprocessor chip with the clip connector. When this connector is connected, a temporary microprocessor stop (TRACE THEN WAIT function) cannot be issued from this unit.

2) 40-pin DIP Plug Connector

This connector can be used when a socket is used for the SUT microprocessor. Disconnect the microprocessor from the SUT socket, connect it to the Microprocessor Probe socket, then insert the plug connector in the SUT microprocessor socket. When this connector is used, the TRACE THEN WAIT function (see 3.2) can be used. Pay close attention to mating the connector pins.

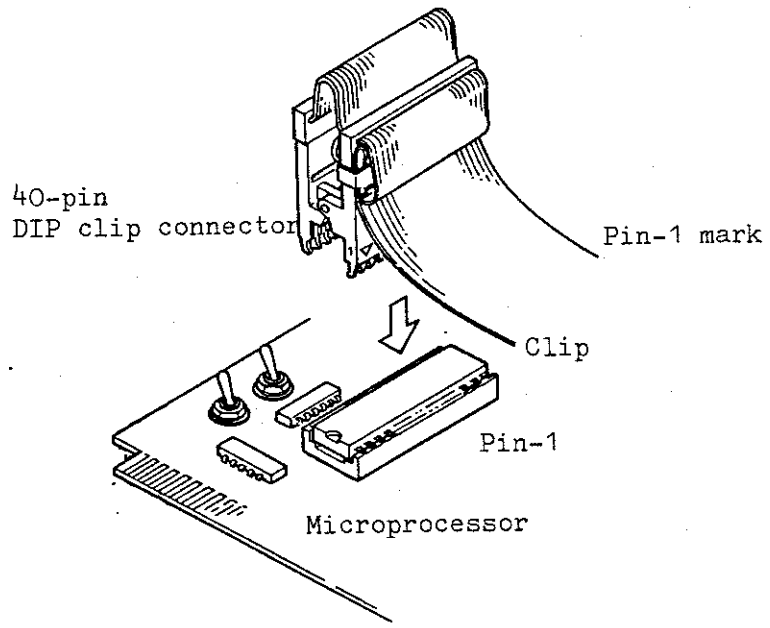


Fig.4 (a) Clip connector in use

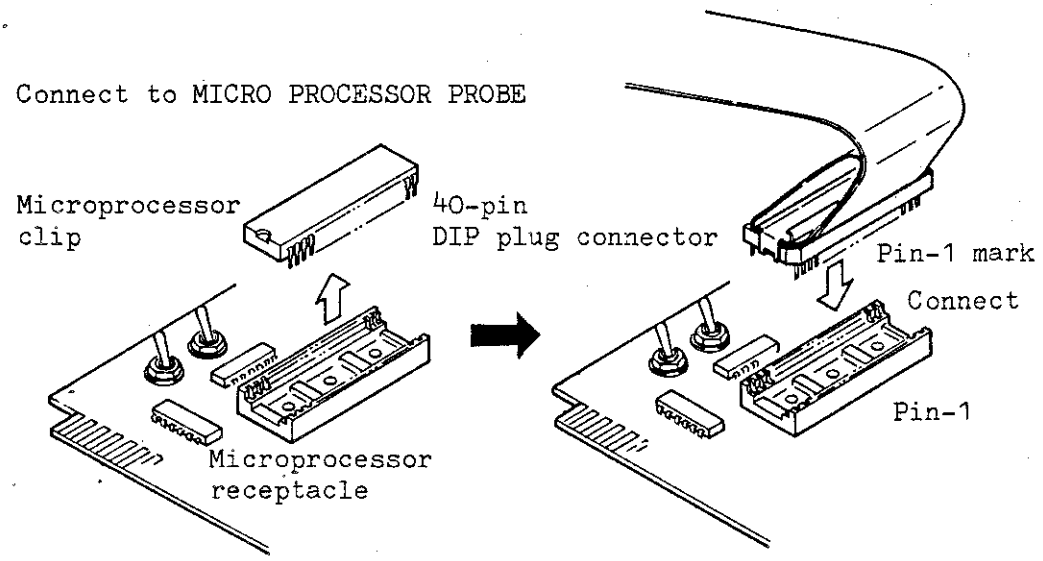


Fig. 4 (b) Plug connector in use

CHAPTER 3

PERSONALITY PANEL OPERATING PROCEDURE

The personality panel comprises the TRIGGER QUALIFIER switches (S1, S2, and S3), TRACE THEN WAIT switch (S4), and CPU STATUS light emitting diodes (LEDs). (See Fig. 5)

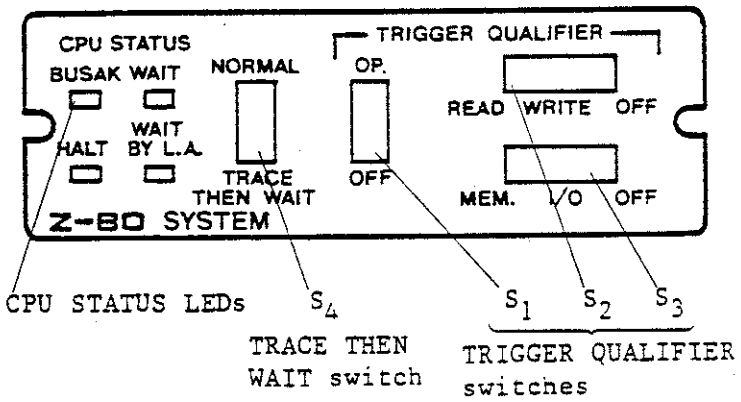


Fig. 5 Personality panel

3.1 TRIGGER QUALIFIER SWITCH OPERATING PROCEDURE

Control signals are fetched together with data in the address and data buses from the microprocessor probe. The personality board decodes these signals and generates the data bus flag to indicate the data type on the data bus, then sends it to the data memory together with the bus data. There are four channels of data bus flags for the Z80 microprocessor to indicate the following:

- Whether bus data is of the fetch cycle (operation code: OP)
- Whether bus data is sent from the memory or I/O units
- Whether bus data is read or write data
- Whether this data is of the second fetch cycle data (OP2)

These flags are decoded with programs in the personality board in the state display mode, then displayed on the CRT display. (See Photo 4 for an absolute display example.) Data bus flag external expressions are displayed on the right side of data bus data. They indicate the following:

1) /OP: Data assumed to be an operation code by the SUT microprocessor.
2) /RD: Data read from the memory (RAM or ROM) to the microprocessor.
3) /WR: Data written from the microprocessor to the memory (RAM).
4) /IN: Data (input data) read from an I/O unit to the microprocessor.
5) /OUT: Data (output data) written from the microprocessor to an I/O unit.
6) /OP2(Note): Second operation code or the last byte in a 4-byte instruction used for an actual operation code.

The trigger qualifier uses those differences of data on the data bus for triggering. When the S1, S2, and S3 switches are all set to OFF, the measurement operation is performed under the trigger conditions specified from the keyboard; however, if at least one of these switches is not set to OFF, the trigger qualifier is operated. All qualifier functions except /OP2 can be added to the trigger conditions by the combination of these switches. The S2 and S3 switch settings are ANDed, then the result is ORed with the S1 switch setting.

Therefore, there are 14 switch combinations for a Z80 microprocessor. (See Table 1) These functions are effective in all measurement modes except the TIME INTERVAL mode and can be used effectively in the TRACE TRIGS mode.

When the S1 switch is set to OFF, the S2 switch to READ or WRITE, and the S3 switch to I/O, only input or output data can be fetched without setting the trigger conditions.

Note: The second operation code is processed in the same way as /OP; however, the operation code in byte 4 is processed in the same way as /RD.

Table 1 Trigger qualifier functions

Trigger qualifier function	S_1	S_2	S_3
/RD recognition	OFF	READ	MEM
/WR recognition	OFF	WRITE	MEM
/IN recognition	OFF	READ	I/O
/OUT recognition	OFF	WRITE	I/O
/RD + /WR recognition	OFF	OFF	MEM
/IN + /OUT recognition	OFF	OFF	I/O
None.	OFF	OFF	OFF
/OP + /RD recognition	OP	READ	MEM
/OP + /WR recognition	OP	WRITE	MEM
/OP + /IN recognition	OP	READ	I/O
/OP + /OUT recognition	OP	WRITE	I/O
/OP + /RD + /WR recognition	OP	OFF	MEM
/OP + /IN + /OUT recognition	OP	OFF	I/O
/OP recognition	OP	OFF	OFF

3.2 TRACE THEN WAIT SWITCH OPERATION

The SUT microprocessor is not interrupted during normal unit operations; however, the program flow can be checked with this switch without interruption. When this switch is used, WAIT(Note) can be issued to the microprocessor after tracing an arbitrary number (1 to 256) of states from the specified trigger point. Thus, the program operation can be checked by dividing it into an arbitrary number of states. (See Fig. 6)

Note: Do not use the TRACE THEN WAIT switch when the dynamic RAM is refreshed with the $\overline{\text{RFSH}}$ pin from Z80.

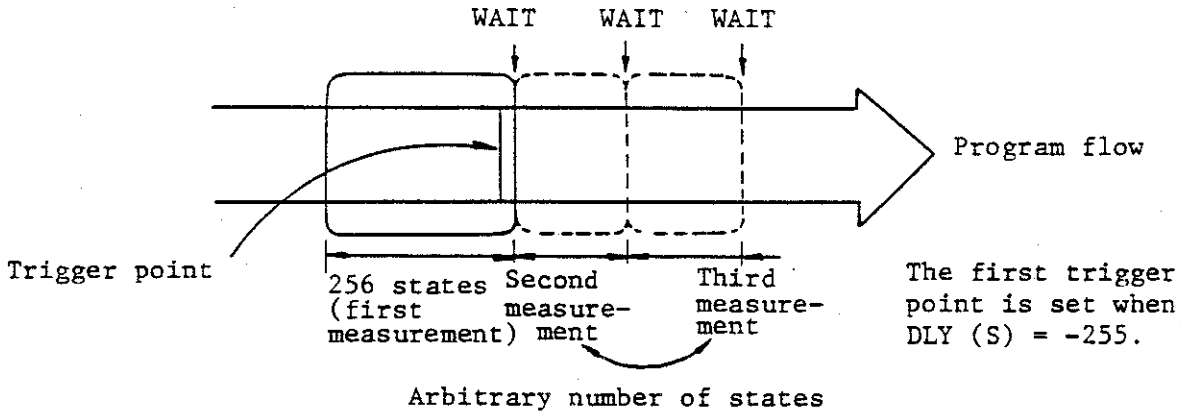


Fig. 6 State analysis with TRACE THEN WAIT switch

Use the TRACE THEN WAIT switch as follows:

1) Since the TRACE THEN WAIT switch can be used only when a 40-pin DIP plug connector is used, disconnect the SUT microprocessor from the socket and insert it to the microprocessor probe socket. Insert a plug connector to the microprocessor socket. (See 2.2 "Microprocessor Connection.")
2) Set the S4 switch to TRACE THEN WAIT, then specify the trace specification from the keyboard. "DLY (S)" can be set arbitrarily; however, when -255 is set, WAIT is issued to the microprocessor immediately after trigger generation during a measurement execution.
3) When the RUN key is pressed, the measurement execution starts and, when the execution is completed by generating a trigger, WAIT is issued. WAIT from the TR4720-540 can be checked with the WAIT BY L.A., one of the CPU STATUS LEDs.
4) When continuous measurement execution is required, set the trace specification set state by the TRACE key, set all trace specifications to "DON'T CARE" by the DEFAULT key, then set "DLY (S)". When "DLY (S)" = 0 is set and data of 256 states is fetched by pressing the RUN key, WAIT occurs. When "DLY (S)" = -n (n = 1 to 255) is set, data of 256 - n states is fetched by pressing the RUN key, then WAIT occurs. When n = 255, a single-state execution is performed.

5) Set the S4 switch to NORMAL to stop the TRACE THEN WAIT function.

3.3 CPU STATUS LED OPERATION

Program execution by the SUT microprocessor can be interrupted with the DMA or multimicroprocessor. Since trace operations are disabled in this state, the microprocessor states are displayed with the following CPU STATUS LEDs:

BUSAK: Goes on when the microprocessor $\overline{\text{BUSAK}}$ signal is low.
HALT: Goes on when the microprocessor $\overline{\text{HALT}}$ signal is low.
WAIT: Goes on when the microprocessor $\overline{\text{WAIT}}$ signal is low.
WAIT BY L.A.: Goes on when the microprocessor WAIT signal is being issued from this unit to the microprocessor.

CHAPTER 4
DATA FETCH AND DISPLAY

4.1 DATA FETCH TIMING

The following data is sampled by the personality board from among the signals sent from the microprocessor:

- Address bus data: 16 channels
- Data bus data: 8 channels
- Data bus flags: 4 channels

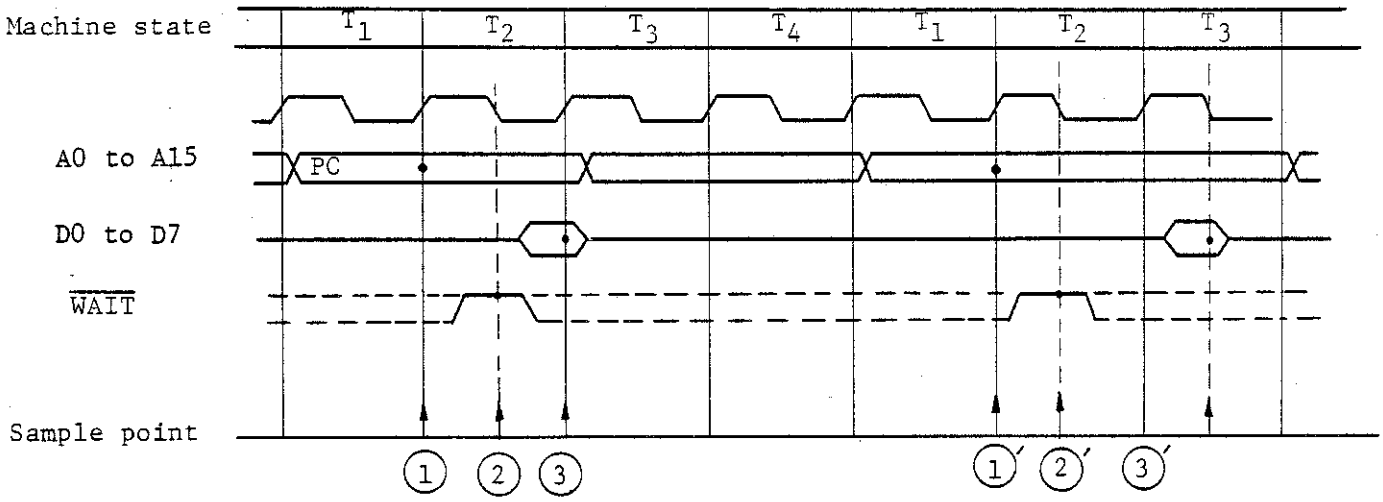
F1 = 1 ($\overline{M1}$ signal is active)
= 0 ($\overline{M1}$ signal is not active)

F2 = 1 ($\overline{IORQ}$ signal is active)
= 0 ($\overline{MREQ}$ signal is active)

F3 = 1 ($\overline{RD}$ signal is active)
= 0 ($\overline{WR}$ signal is active)

F4 = 1 ($\overline{M1}$ signal is active in the second fetch cycle; or $\overline{M1}$ signal is not active but the last byte in a 4-byte instruction is an actual operation code)
= 0 (Other than above)

The above data is sampled with the sampling clocks generated from the microprocessor control signals. (See Fig. 7)



This example shows the operation code fetch cycle and data read cycle.

1) Operation code fetch(Note)
   1 Address bus is sampled with $\phi\uparrow$ of T_2.
   2 $\overline{WAIT}$ signal is checked with $\phi\downarrow$ of T_2 or T_W (wait machine state).
   3 Data bus and data bus flags are sampled with $\phi\uparrow$ of T_3.

2) Data read or write
   ①' Address bus is sampled with $\phi\uparrow$ of T_2.
   ②' $\overline{WAIT}$ signal is checked with $\phi\downarrow$ of T_2 or T_W.
   ③' Data bus and data bus flags are sampled with $\phi\downarrow$ of T_3.

Note: The operations are the same as those when an operation code is inserted from an external unit as interruption.

•: Sample point
|: Leading edge
|: Trailing edge

Fig. 7 Data sampling timing in personality board

4.2 FETCHED DATA DISPLAY

4.2.1 Disassembly Format

1) The ZILOG Z80 standard assembly format is used for the operation code mnemonics. (Refer to the Z80 Assembly Language Programming Manual.)

2) All operand data (one or two bytes) is displayed in hexadecimal notation. Therefore, symbols indicating the numeric base are not used.

   Example: LD A, 10H ←——— LD A,10
   (ZILOG format) (TR4720 format)

3) When there is an operation code and there is no operand in the data memory, the operand is displayed as "+++".

   Example: When the last state in the data memory is displayed as 3E/OP with absolute display, "LD A, +++" is displayed with mnemonic display.

4) Z80 has a relative addressing mode (JR or DJNZ); in this case, the address is converted into an absolute address internally, then displayed.

   Example: JR & 1234 (& indicates relative addressing)

5) Parentheses ( ) are not used when a port is specified with numerals in an I/O instruction.

   Example: IN A, (OCCH) ←——— IN A, CC
   (ZILOG format) (TR4720 format)

6) Formats of instructions specifying an interrupt mode are different.

   IM 0 - IM 2 ←——— IM0 - IM2
   (ZILOG format) (TR4720 format)

7) A blank may be displayed for an unexisting operation code; in this case, observe in the absolute display.

4.2.2 Display by Special Microprocessor Operation

1) "HALT"

   Even when a "HALT" instruction is executed, the Z80 is not stopped because an $\overline{RFSH}$ signal is sent and continues executing an "NOP" instruction.

Since the machine cycle is apparently equivalent to fetching the instruction at the address following the HALT instruction, the instruction code is displayed continuously.

2) Nonmaskable interrupt

The return destination address is written in the stack; then control is transferred to 66H.

Example:

[ADRS]	[DATA]	
FFFF	12 /WR	Stack write
FFFF	34 /WR	
0066	3E /OP	Interrupt routine

3) Maskable interrupt

"Mode 0": The data bus flag of the operation code inserted from an external unit is /IN.

Examples: 1. When "RST 30" instruction is inserted

[ADRS]	[DATA](Note)	
1234	F7 /IN	Operation code inserted from an external unit
FFFF	12 /WR	Stack write
FFFE	34 /WR	
0030	3E /OP	Interrupt routine

2. When "CALL 5678" instruction is inserted

[ADRS]	[DATA](Note)	
1234	CD /IN	instructions inserted from an external unit
1234	78 /RD	
1234	56 /RD	
FFFF	12 /WR	Stack write
FFFE	34 /WR	
5678	3E /OP	Interrupt routine

Note: Since F1 = F2 = F3 = 1, this data is processed as an operation code in a mnemonic display.

"Mode 1": The format is the same as that in mode 0; however, inserted data is meaningless.

Example:

[ADRS]	[DATA]	
1234	FF /IN(Note)	Meaningless data
FFFF	12 /WR	Stack write
FFFE	34 /WR	
0038	3E /OP	Interrupt routine

Note: Though this data is meaningless, this is processed as an operation code in mnemonic display because F1= F2 = F3 = 1, and "RST 38" is displayed.

"Mode 2": Data (interrupt routine address low-order byte), not an operation code, is inserted from an external unit; this is displayed as an operation code in mnemonic display.

Example:

[ADRS]	[DATA]	
1234	FF /IN	Data to be inserted
FFFF	12 /WR	Stack write
FFFE	34 /WR	
01FF	78 /RD	Interrupt routine address read
0200	56 /RD	
5678	3E /OP	Interrupt routine

4) Bus and control signals float in the BUSAK state and data is not sampled.

CHAPTER 5
OPERATION CHECK

There are many connectors and IC connections between the data fetching point at the MICROPROCESSOR PROBE tip and the data memory in the TR4720. Therefore, the personality board has a test pattern generator corresponding to the microprocessor bus and control signals to fetch correct data and test patterns are output to the CPU PROBE TEST receptacle on the rear panel. Whether the route between the probe tip and data memory is operating normally can be checked with these test patterns. Check the route as follows:

1) Connect a 40-pin DIP clip connector or 40-pin DIP plug connector to the MICROPROCESSOR PROBE.
2) When a plug connector is used, connect it directly to the CPU PROBE TEST receptacle; when a clip connector is used, connect the MICROPROCESSOR PROBE via the attached 40-pin DIP IC package.
3) Set the "TRACE STATE ALL" mode with the TRACE key, then initialize all trace specifications by pressing the DEFAULT key.
4) Since the input prompt is located at "TRIG-[ADRS]", input "0000" with the ENTRY keys.
5) When the RUN key is pressed, test patterns (see Photo 5) are displayed. Check that the same digits are displayed for data on the address and data buses.
6) If required, other basic functional operations can be checked.

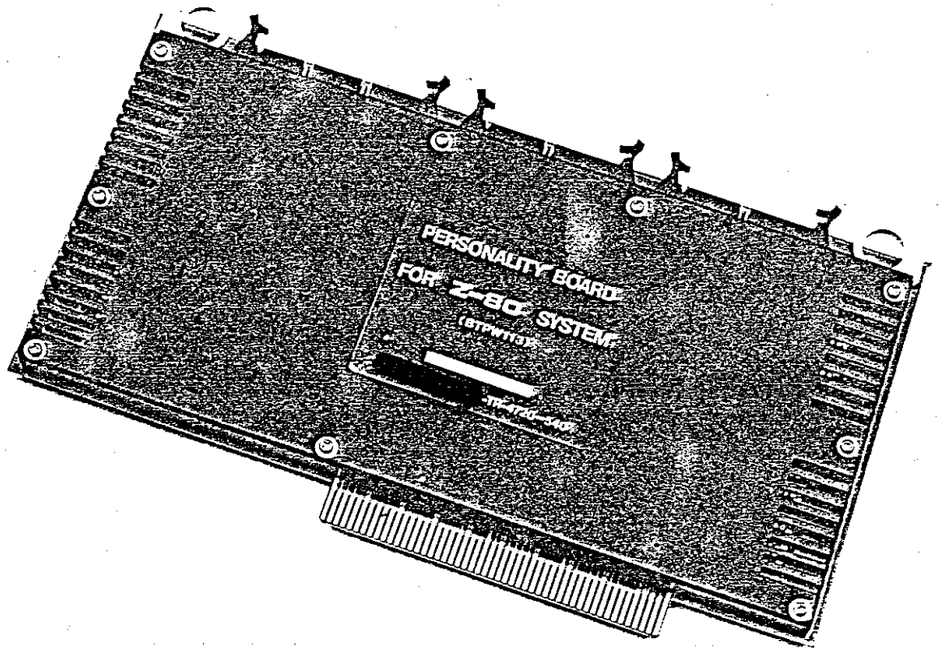


Photo 1 Personality board

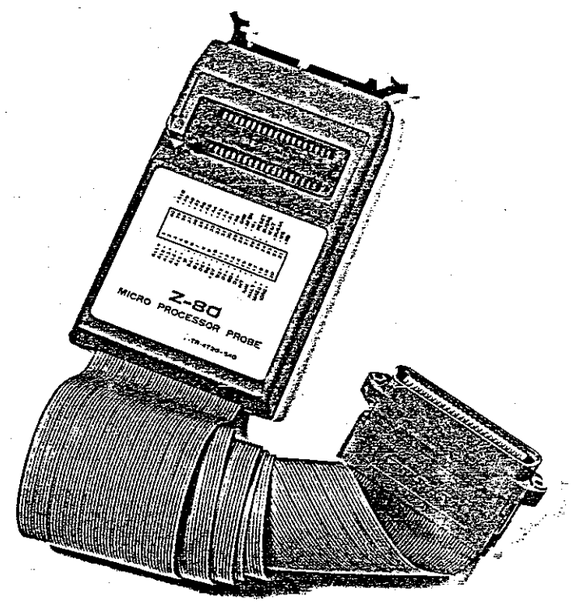
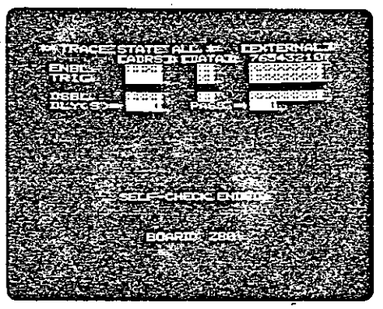


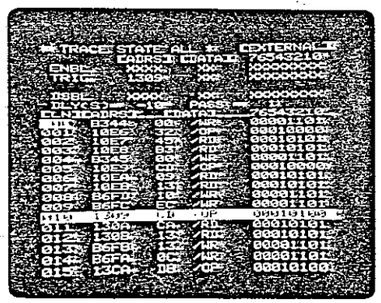
Photo 2 MICRO PROCESSOR PROBE

Photo 3



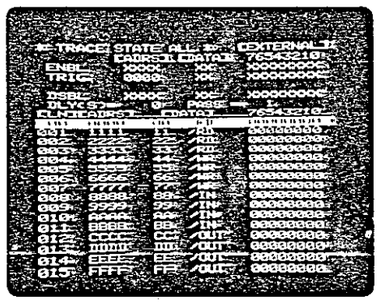
Personality board identifier display at power on

Photo 4



ABS mode display (TRACE STATE ALL)

Photo 5



Test patterns

CHAPTER 6
PRINCIPLES OF HARDWARE OPERATION

6.1 GENERAL

This chapter, prepared for electronic engineers, explains the configuration and operation principles of the TR4720-540 Z80 Personality Kit. (See also the detailed circuit diagrams and parts list in the block of this manual.)

(Refer to the 7.2 "Signal Names" and Appendix in the TR4720 Logic Analyzer Instructions Manual for terms and signal names.)

6.2 PERSONALITY BOARD (PW115) FUNCTION OUTLINE

The Z80 Personality Board (PW115) comprises the following circuits. (See Fig. 6.1 for the block diagram.)

1) Sampling clock generator and latch circuit for data (address and data) fetched via the microprocessor probe.
2) Instruction decoder (OP2) and data bus flag (SF0L to SF3L) generator circuits for data fetched via the microprocessor probe.
3) Decoder circuit for the CPU status fetched via the microprocessor probe. (LED display signals are generated.)
4) ROM for disassemble processing.
5) Pattern signal generator circuit for microprocessor probe test.
6) Wait signal generator circuit for TRACE THEN WAIT function.
7) Sampling clock switching circuit for state and timing displays.

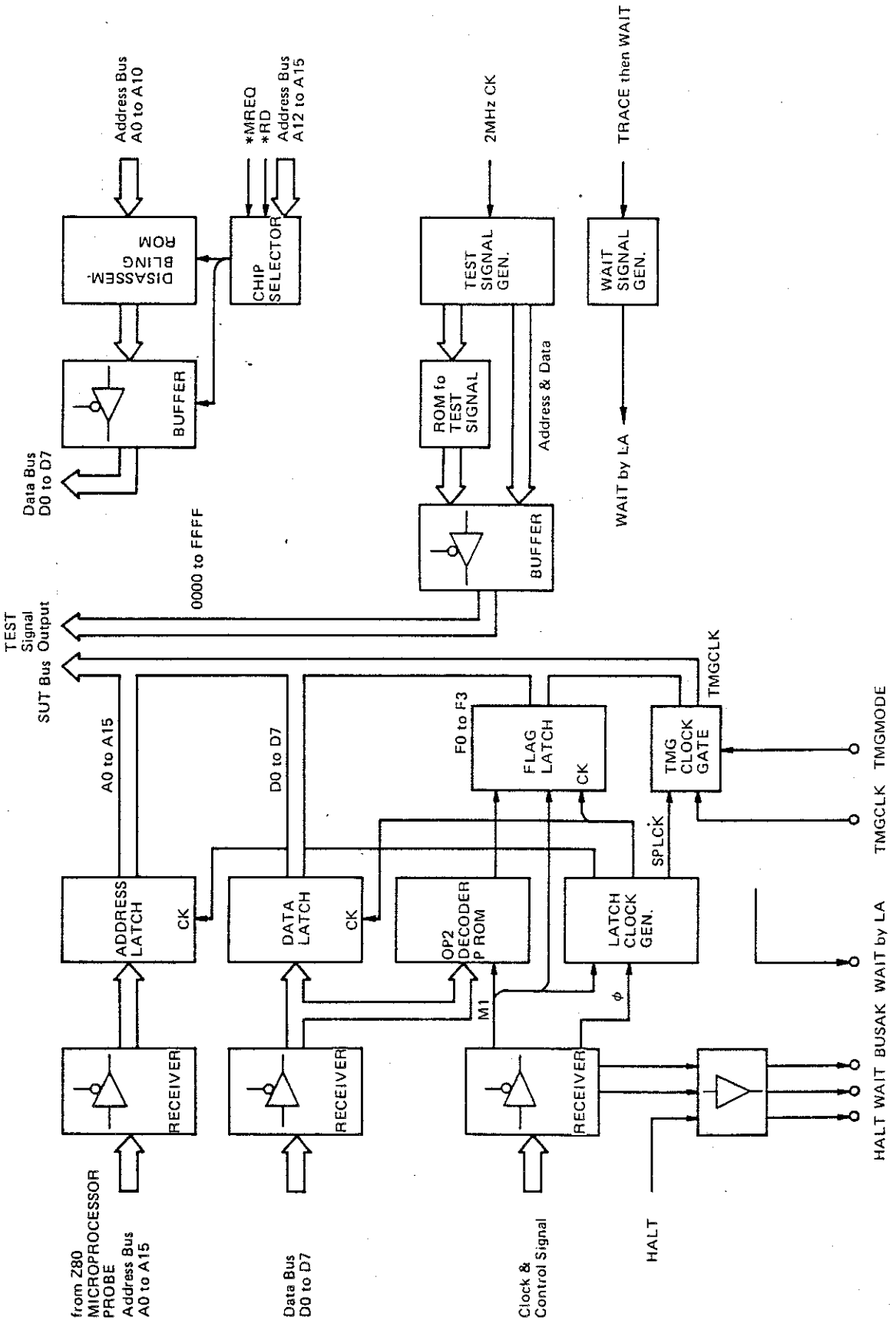


Fig. 6.1 Z80 Personality Board (PW113) block diagram

6.3 SAMPLING (LATCH) CLOCK GENERATOR CIRCUIT

Operation principles:

1) Data sampling is performed in the order of the address sampling (FF1 output), wait check (FF3 output), and data sampling (FF2 output).
2) When MREQ OR IORQ is effective (low level), the address latch signal flip-flop (FF1-Q) goes to high level at the leading edge of the next clock ϕ to latch address data. The wait check flip-flop (FF3) clear and presetting of the wait off hold flip-flop (FF4) are reset.
3) After step (2) above, wait check is performed at the trailing edge of the next clock ϕ.
4) When the wait state goes to low level, the data latch signal flip-flop (FF2) is inhibited while maintaining the wait check flip-flop (FF3-Q) at low level.
5) When the wait state goes to high level and is cleared, the wait check flip-flop (FF3-Q) goes to high level and inhibition of the data latch signal flip-flop (FF2) is reset.
   The wait off hold flip-flop (FF4-Q) goes to low level and the wait state is cleared.
6) At the leading edge of the next clock after clearing the wait state, the data latch signal flip-flop (FF2-Q) goes to high level and the data and status (flag) are latched.
7) When MREQ or IORQ signal is made ineffective or a BUSAK or RFSH signal is received, FF1 is cleared and the sampling clock generaator circuit is initialized.
8) See Fig. 6.2 for the latch clock generator circuit and Fig. 6.3 for the data sampling timing chart.

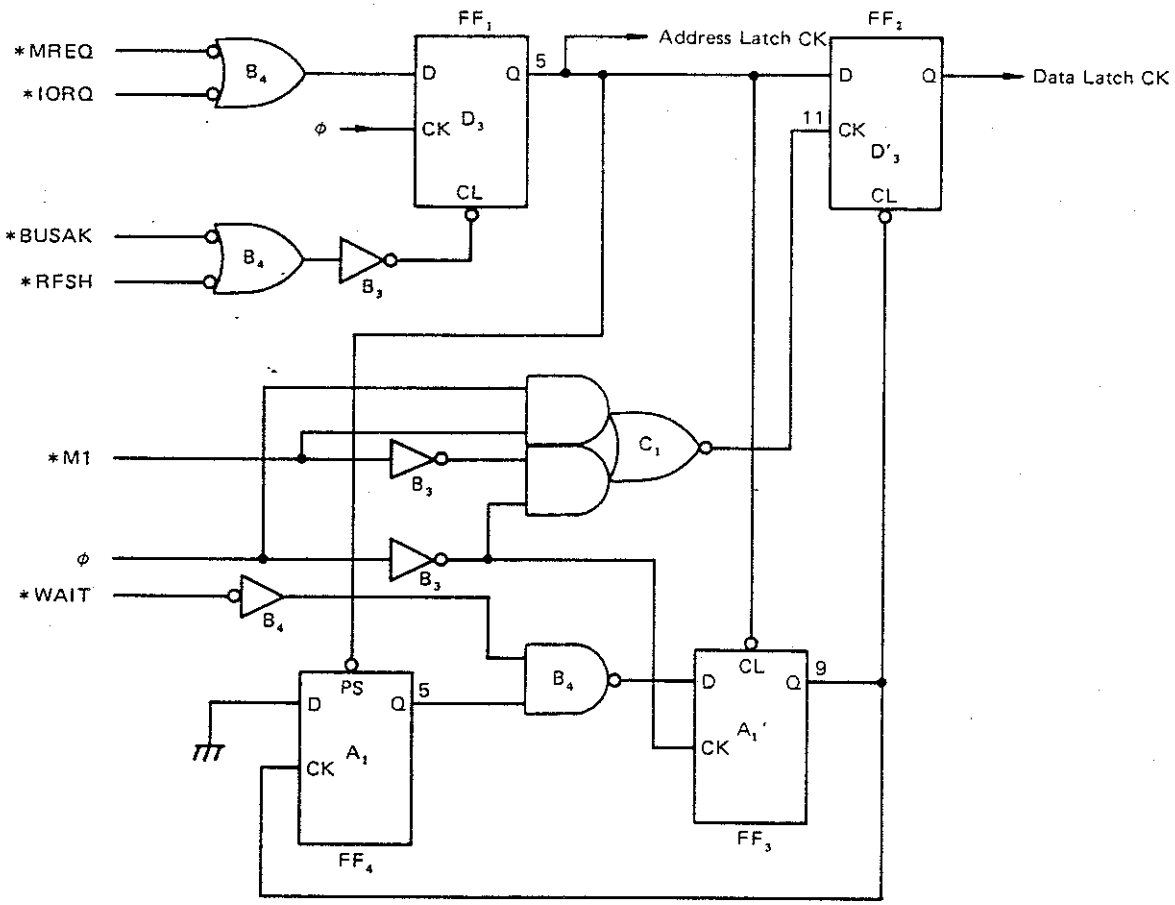


Fig. 6.2 Latch clock generator circuit

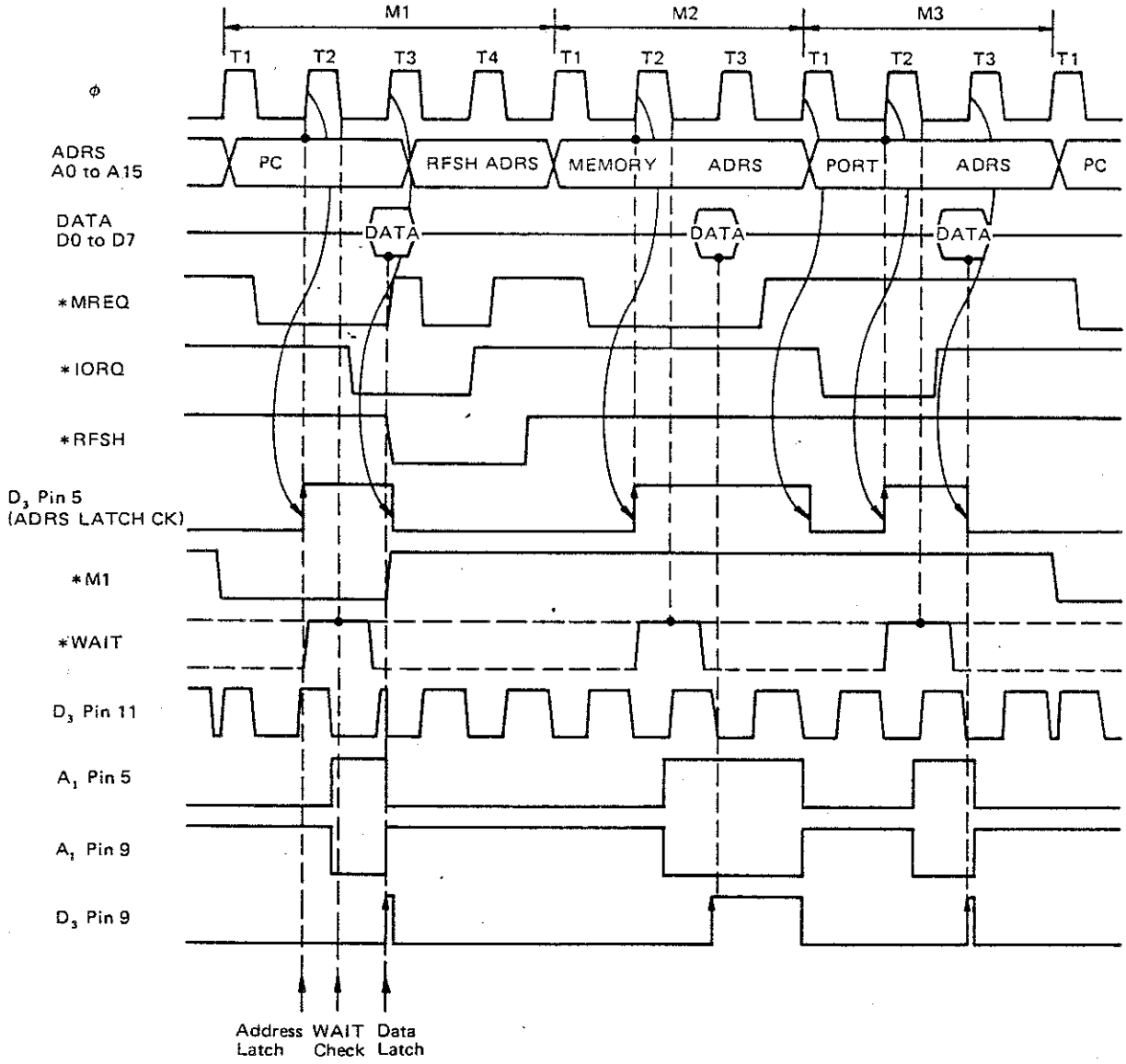
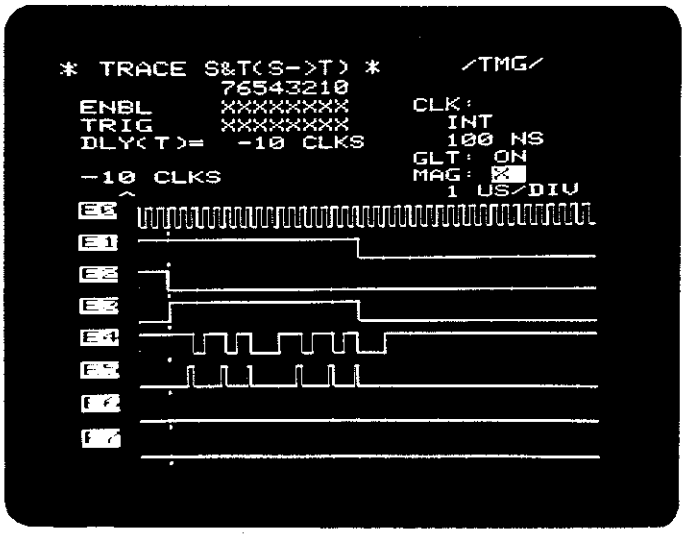


Fig. 6.3 Sampling (latch) timing chart



E_0: B_5 Pin 4 (ϕ)
E_1: E_2 Pin10 (*DLY OVER FLOW)
E_2: D_1 Pin 5 (CTR INH)
E_3: E_2 Pin 6 (*WAIT BY LA)
E_4: D_4 Pin11 (ADDR Latch CK)
E_5: A_4 Pin11 (DATA Latch CK)
E_6: D_1 Pin 1 (NOT TRACE)
E_7: D_1 Pin 3 (*TRACE then WAIT)

Fig. 6.4 WAIT BY LA timing example (DLY(S) = -250 clocks)

6.4 OP2 DECODER CIRCUIT

In Z80, some codes are used as expansion words and the subsequent codes are used as actual instruction codes to expand instructions. There are four 2-byte instruction codes in these expansion words: FD, DD, CB, and ED

An OP code succeeds the above instruction codes; this is allocated to flag F3 as OP2.

OP OP2
Two-byte instruction example: PUSH IY:FD E5

If byte 4 is the OP code (for example in continuous instruction codes such as DD•CB and FD•CB), bytes 2 and 4 are used as OP2.

Mnemonic code OP OP2 OP2
Four-byte instruction example: SET b, (IY + d): FD CB ← d → 11 b 110
(d is read as data.)

(See Fig. 6.5 for the OP2 flag generator circuit.)

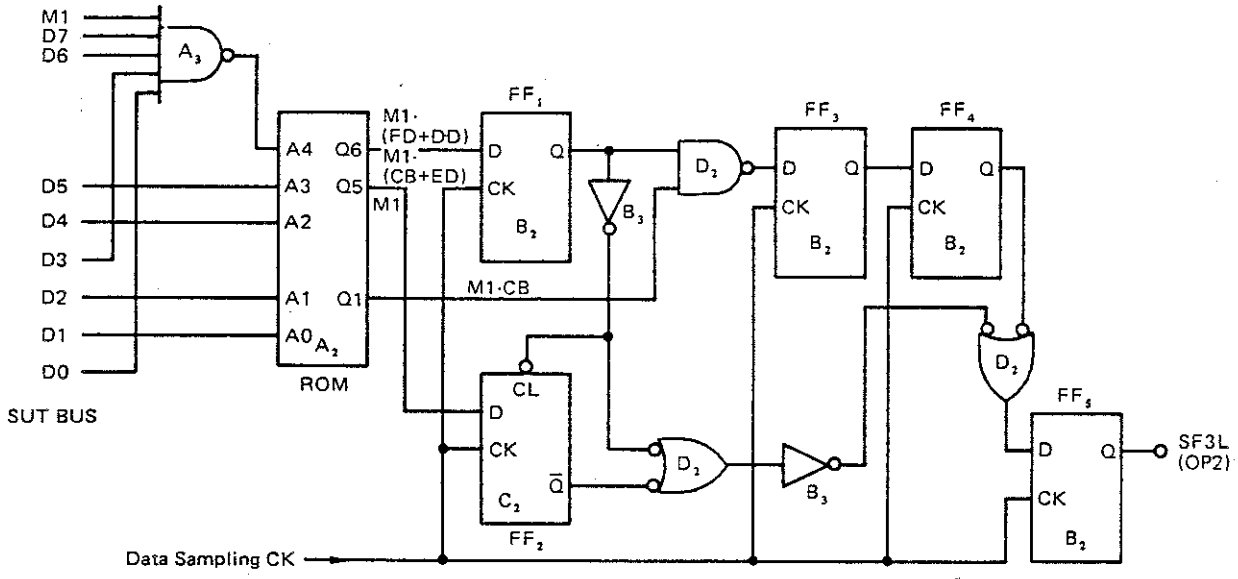


Fig. 6.5 OP2 decoder circuit

Operation principles:

1) Data from the SUT bus is decoded with ROM (A2) in the M1 cycle (OP code fetch cycle) and output as M1•CB, M1•(CB + ED), or M1•(FD + DD).
2) If the decoder output is (CB + ED), it is latched by FF2. It is further latched by FF5 in the data sampling clock of byte 2 and F3 ("1") is output. This F3 output indicates that byte 2 is OP2.
3) If the decoder output is (FD + DD), it is latched by FF1. It is further latched by FF5 at the data sampling clock of byte 2, and F3 is output.
4) If the FF1 output goes to high level, gate (D2) opens; if byte 2 is CB, data is latched by FF3 in the data sampling clock of byte 2 via this gate (D2). It is further latched by FF4 at the data sampling clock of byte 3, then latched by FF5 at the data sampling clock of byte 4 to output F3. This F3 output indicates that byte 4 is OP2.

6.5 DATA BUS FLAG CIRCUIT

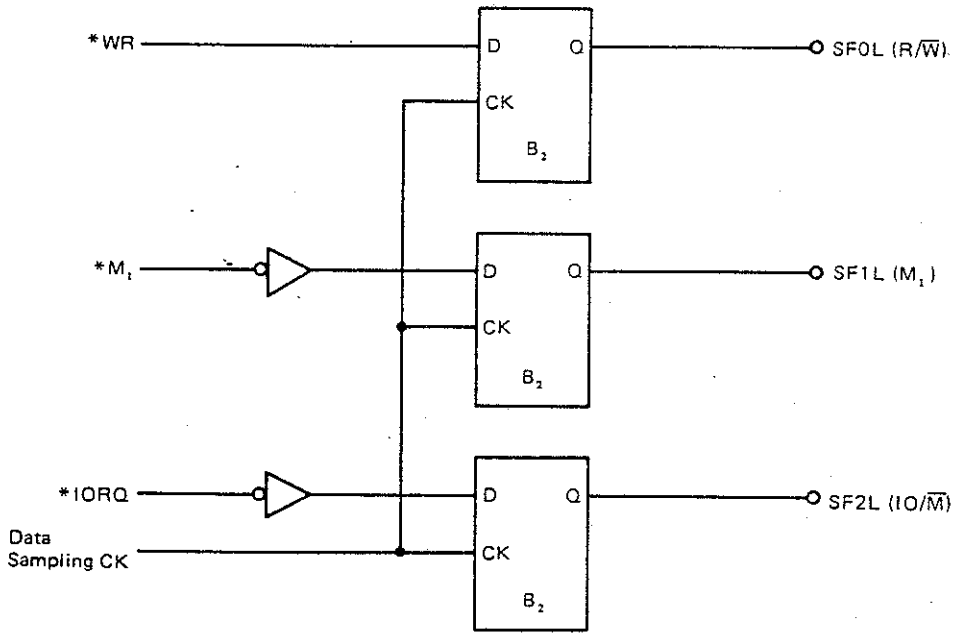


Fig. 6.6 Data bus flag circuit

6.6 MICROPROCESSOR PROBE TEST OUTPUT SIGNAL GENERATOR CIRCUIT

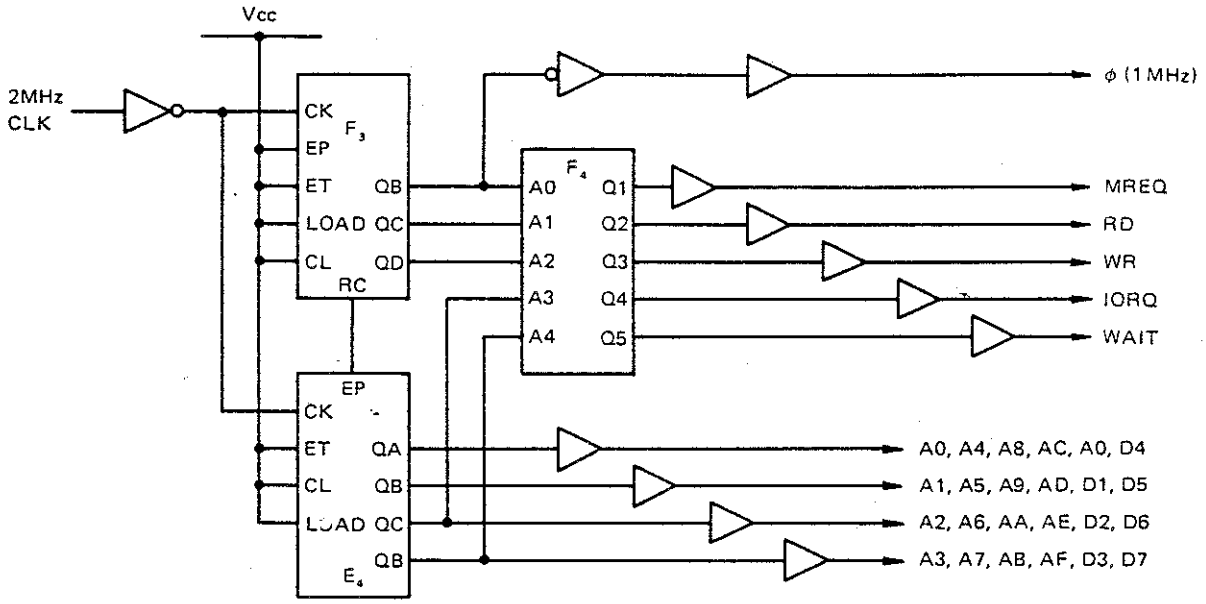


Fig. 6.7 Test signal generator circuit

The program for the control signal ROM. Checks 16 states per cycle (1 to F) and divides them into four states: RD, WR, IN, and OUT. Eight clocks are used in one state.

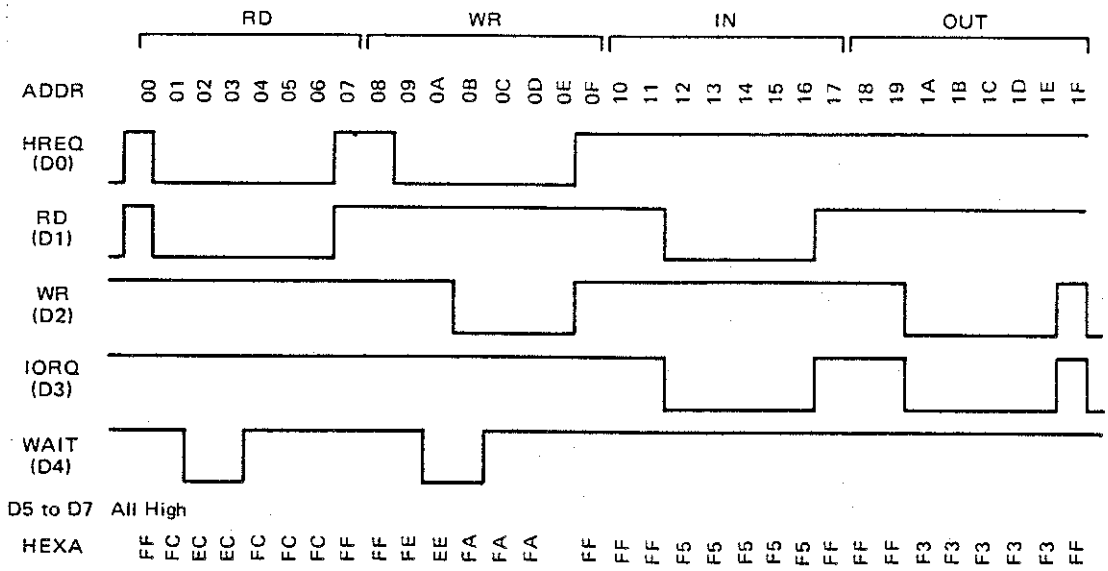


Fig. 6.8 Control signal bit allocation

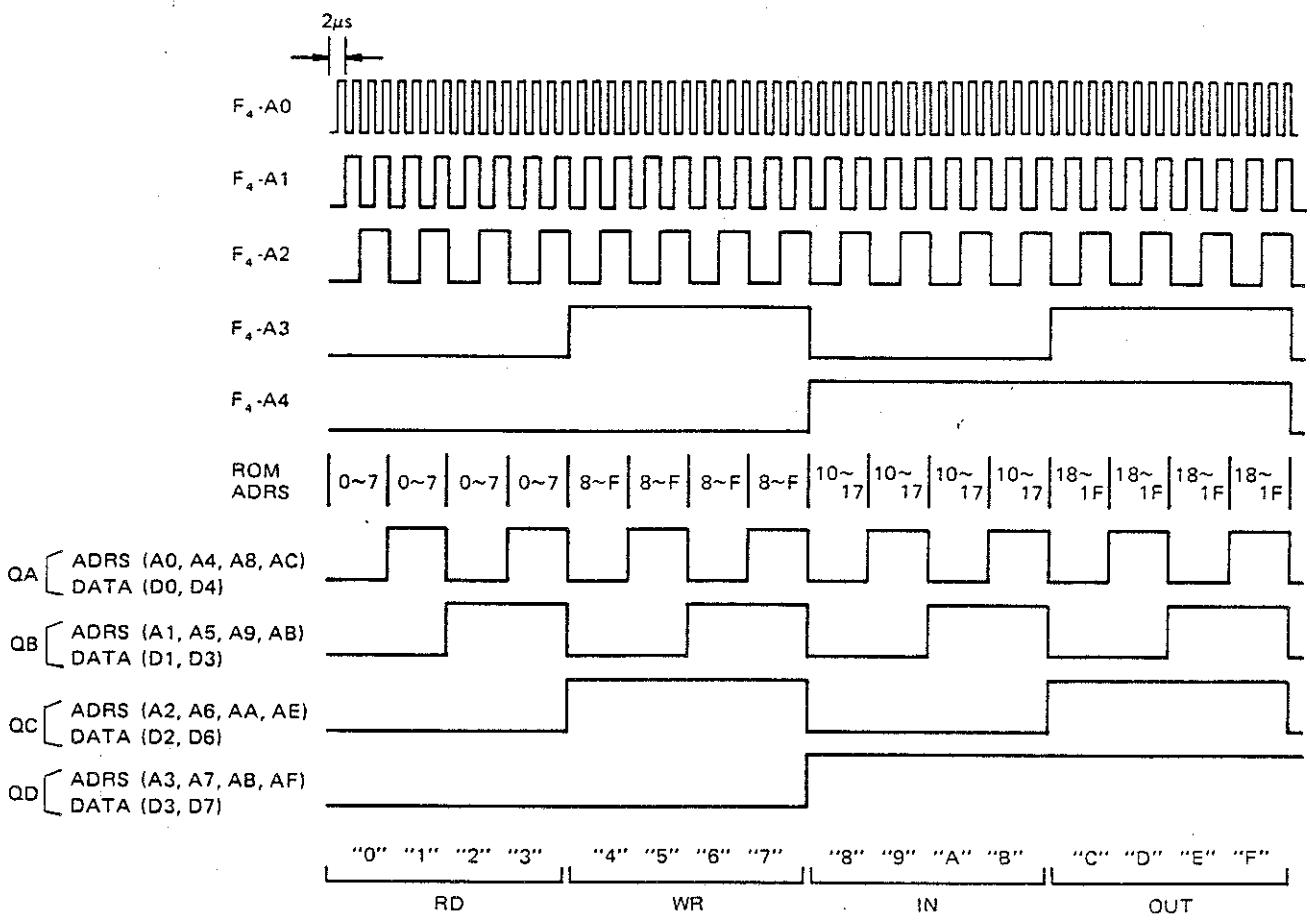


Fig. 6.9 Test signal output timing chart

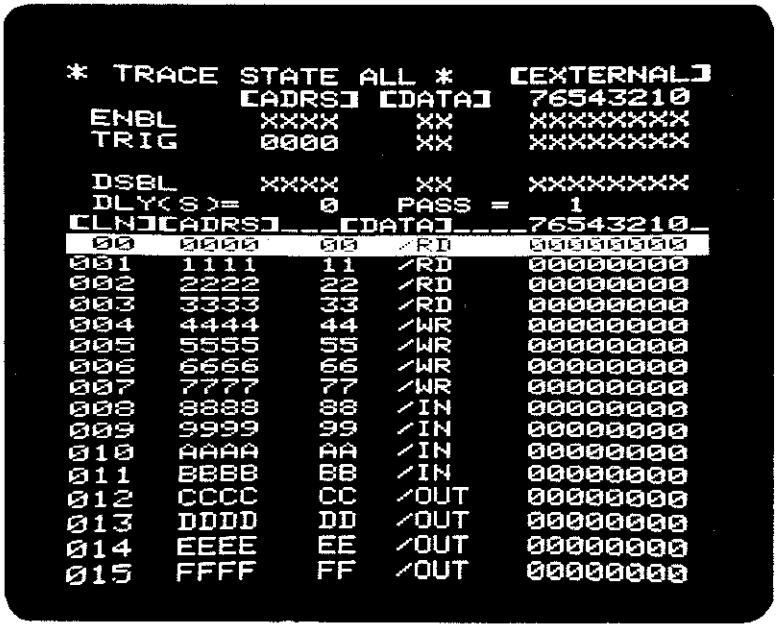


Fig. 6.10 Test pattern

6.7 STATUS DISPLAY

1) HALT

While the CPU executes a *HALT instruction (the CPU stops), this signal sets the HALT lamp on the panel to ON.

2) WAIT

When the CPU is set in the temporary wait state by a *WAIT signal, this signal sets the WAIT lamp on the panel to ON.

3) BUSAK

When the CPU address bus, data bus, and three state control signal are set in the high-impedance state, this signal sets the BUSAK lamp on the panel to ON.

4) *WAIT BY LA

When a WAIT signal is issued from the TR4720 to the microprocessor, this signal sets the WAIT BY L.A. lamp on the panel to ON. This lamp goes on only when the switch on the panel is set to TRACE TEN WAIT.

6.8 TRACE THEN WAIT CIRCUIT

This circuit is actuated only when TRACE is selected; it temporarily stops the CPU operation on the SUT side when DLY1 CNT overflows (the CPU enters the wait state).

The program flow can be checked continuously by this function.

Programs can be executed in single steps by setting TRIG to DON'T CARE and DLY(S) to -255 clocks.

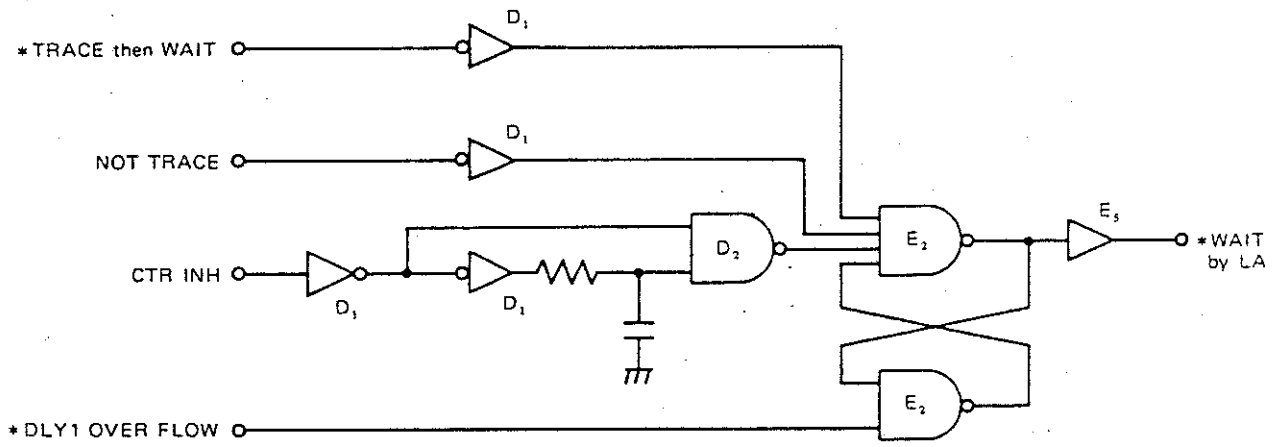


Fig. 6.11 TRACE THEN WAIT circuit

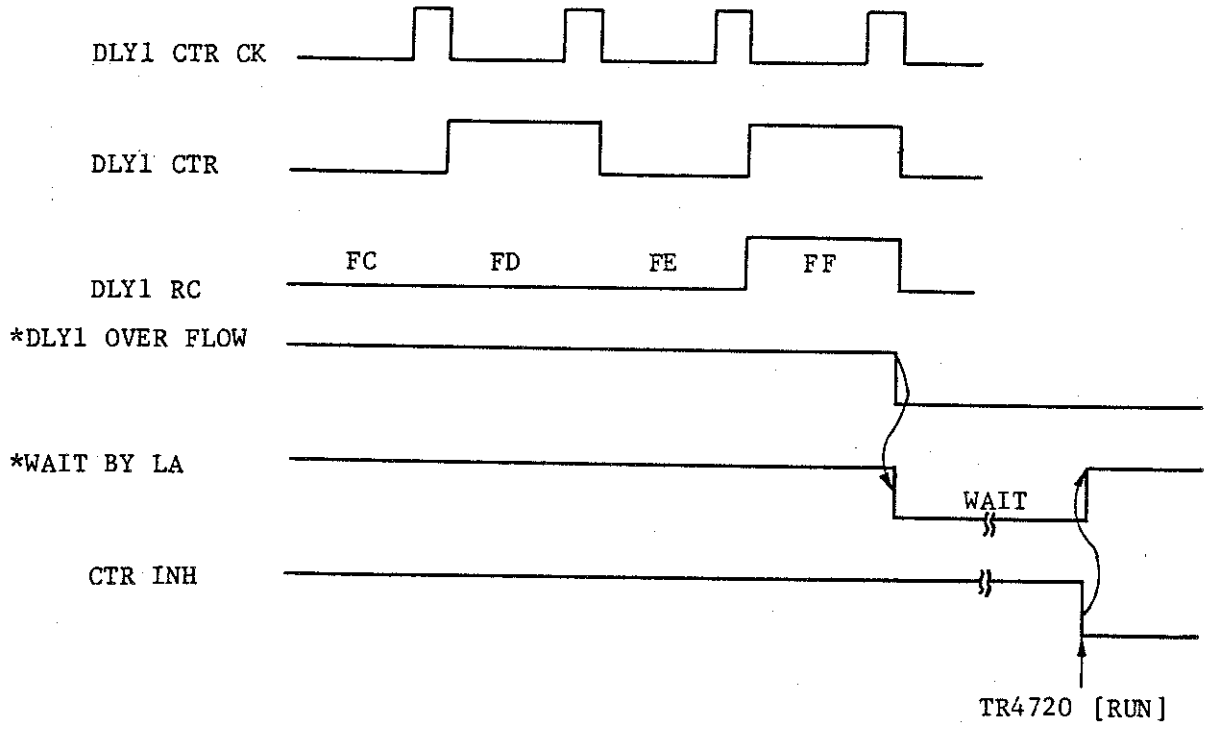


Fig. 6.12 TRACE THEN WAIT function timing chart

CHAPTER 7
SOFTWARE EXPLANATION

7.1 GENERAL

All software functions that depend on various microprocessors to be tested are on the personality board of the TR4720 Logic Analyzer; thus, the TR4720 can be measure various microprocessors.
The program in this board is called personality program (ROM2).
The roles of the personality program are to analyze data on the SUT data bus in the high-speed memory (HSM) (data type analysis and disassembling), convert it to the specified format, then display it on the CRT display.

7.2 PERSONALITY PROGRAM (ROM2) ROLES

7.2.1 Personality Board Identifier Display

The personality board cannot be seen from outside; when the POWER switch is set to ON, the identifier (object microprocessor name) is displayed on the CRT display. The identifier is written in 6-bit ASCII code after address 3003_H.

7.2.2 SUT Data Bus Data Display

If a return instruction is stored at addresses $300A_H$ and $300D_H$, ROM2 is used as one of the ROM1 subroutines.
SUT data is stored in the high-speed memory (HSM) at the end of measurements; it is read with the ROM1 display routine, then displayed on the CRT display in the predetermined format (address in four hexadecimal digits, data in two hexadecimal digits, and mnemonic and external codes in eight binary digits). (See Fig. 7.1 for the data display flowchart.)
Of the above data, only data bus data is converted and displayed by ROM2. ROM2 is called only once for one display line; it returns to ROM1 when display is completed.
There are two display modes:

1) Absolute mode

SUT data is displayed as two hexadecimal digits; the data type (OP, RD, WR, IN, OUT, and so forth) is displayed in the next field.

2) Mnemonic mode

Disassemble display is performed using the OP code fetch cycle as a key. The format is the same as those for other microprocessors.

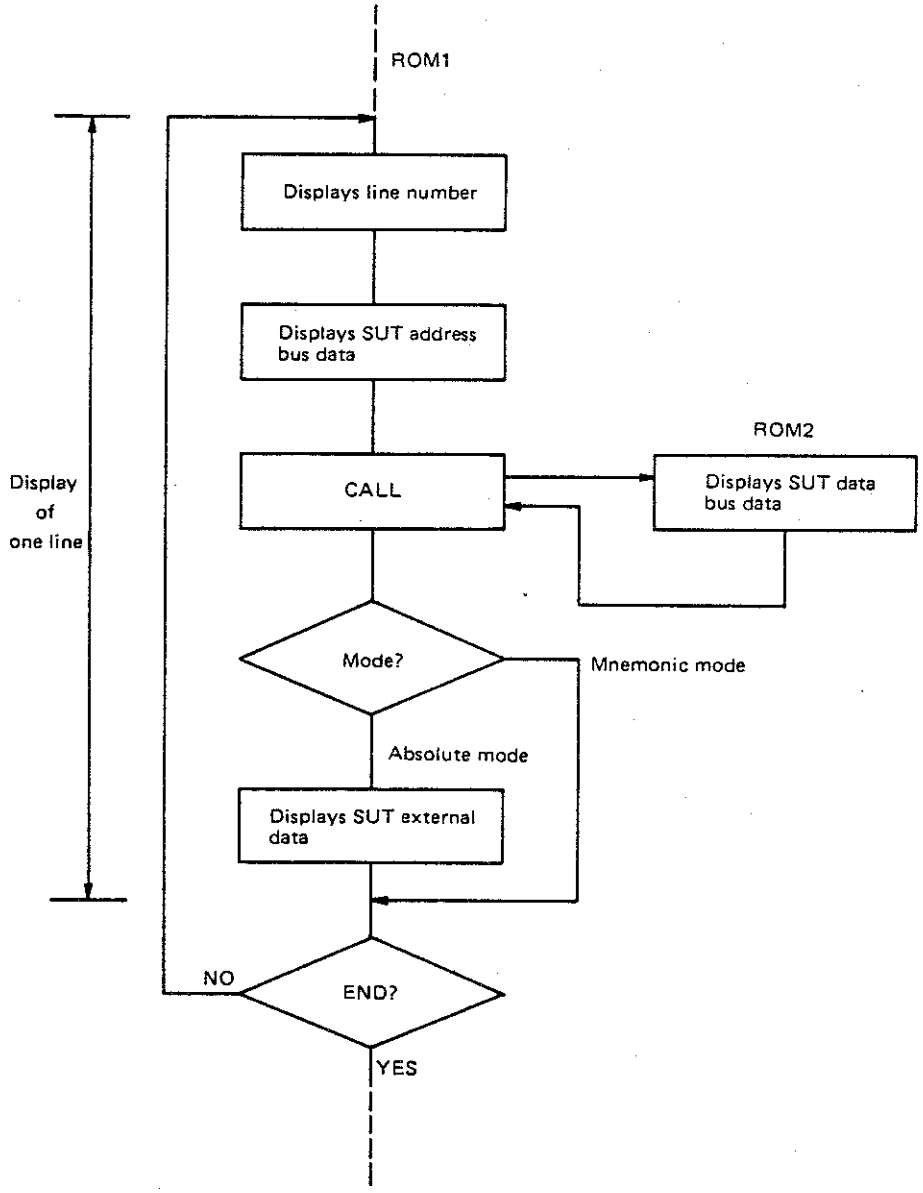


Fig. 7.1 Data display flowchart

7.3 RESOURCES REFERENCED FROM PERSONALITY PROGRAM (ROM2)

Five resources are necessary to realize the ROM2 function:

① HSM-DATA: SUT data bus data

② HSM-FLAG: SUT data bus flag

③ MACS: HSM address counter (eight bits)

④ V-RAM: Video RAM (1 to 1 correspondence with CRT display)

⑤ T-RAM: Temporary RAM (temporary memory for data and status)

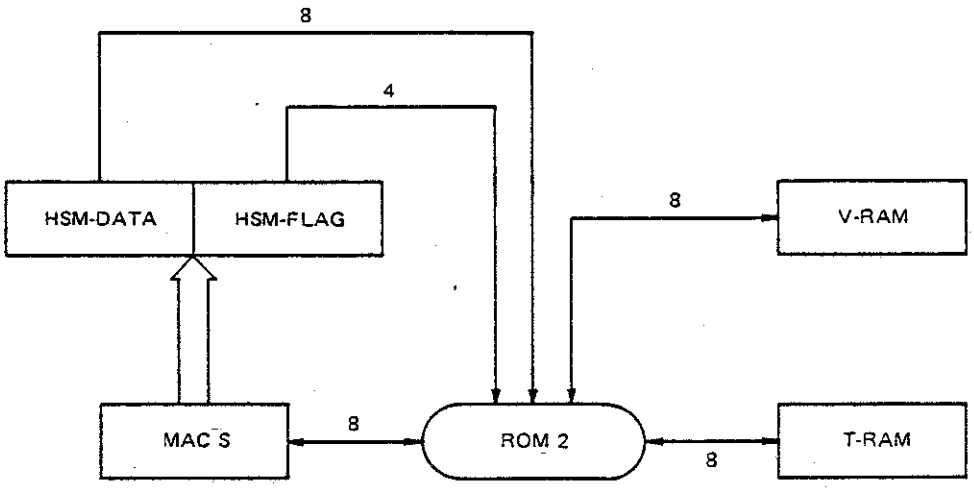


Fig. 7.2

① HSM-DATA (port address: HSM DAT)

Read-only port.

② HSM-FLAG (port address: HSM FLG)

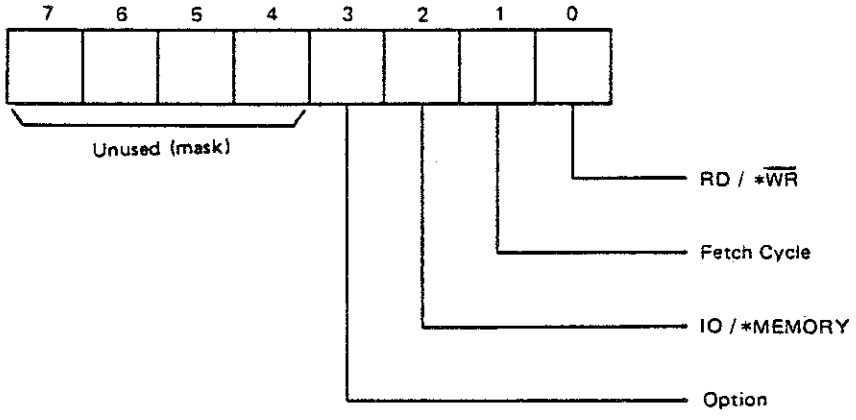


Fig. 7.3

Data of bl = "1" is used as a key for disassembling.
Data types are analyzed with these flags.

③ MACS (port address: MACS)

Since the HSM has 256 words, it requires an 8-bit counter. MACS must be specified to read HSM data. The MACS value can be read by port read (00_H to FF_H) and MACS is incremented by port write.

④ V-RAM (memory address: $B000_H$ to $B2FF_H$)

ROM2 can be used in the area shown in Fig. 7.4. One word comprises an ASCII code (six bits) and control flags (two bits).

Four character display modes can be specified by a combination of the control flags.

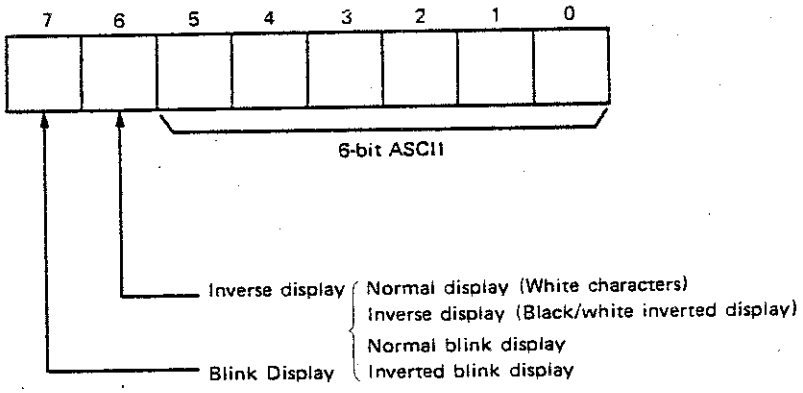


Fig. 7.4

5 T-RAM (memory address: $B300_H$ to $B7FF_H$)

The T-RAM, set from the keyboard, holds the current display mode.
Only bit 0 is necessary for ROM2.

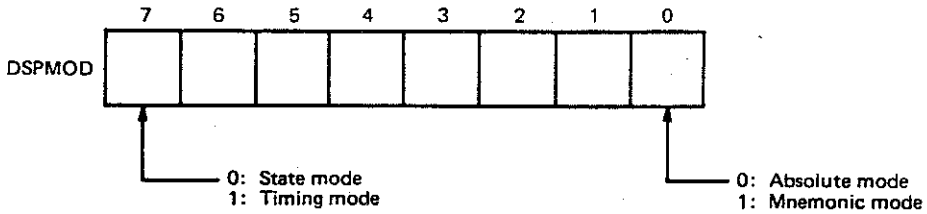


Fig. 7.5

Display area accessible by personality program

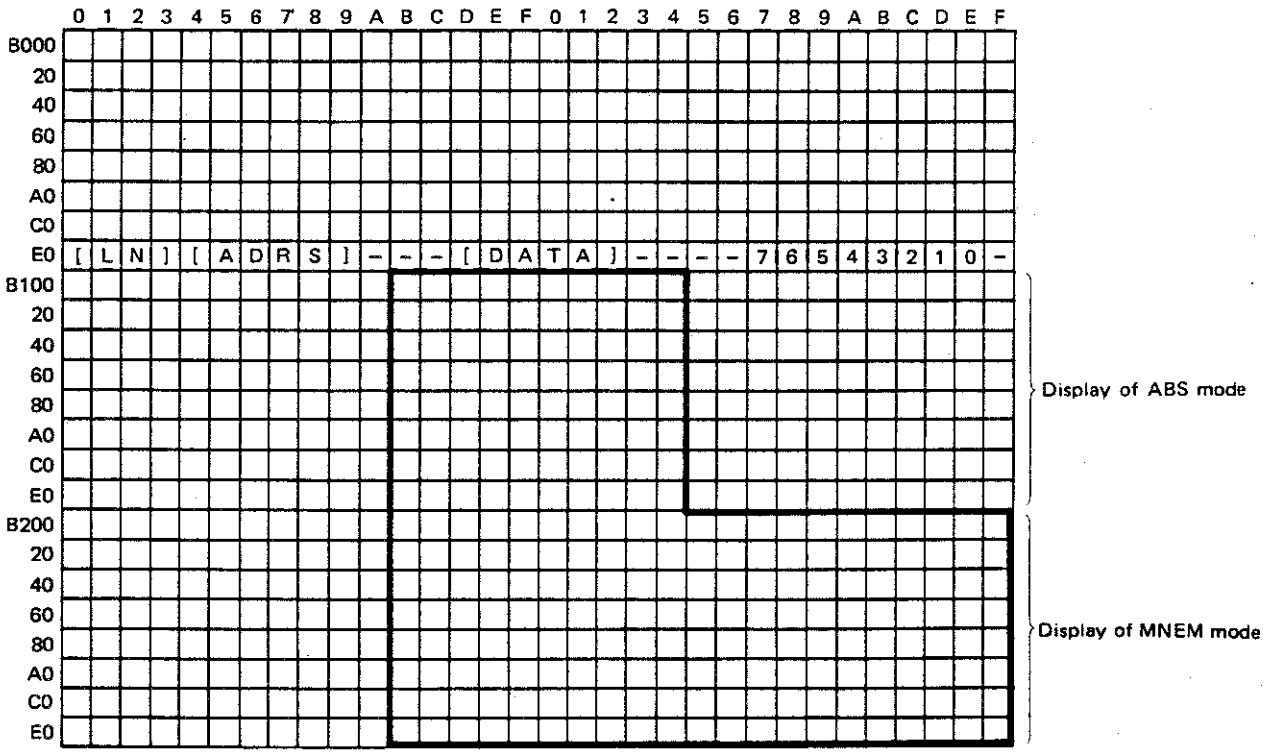


Fig. 7.6 TR4720 Video RAM layout

7.4 PERSONALITY PROGRAM (ROM2) CONFIGURATION

ROM2 comprises four blocks:

1) HEADER: Information block for data linking and control passing between the personality program and other resources.
2) TABLE: Blcok for mnemonic and other tables. This block is used to generate the absolute address table.
3) PROGRAM: Program block for the personality program.
4) SUBROUTINE: Block in which common subroutines used for execution of the personality program are gathered.

   Subroutines:

   a) HEX 2AS: Converts an 8-bit binary number (two hexadecimal digits) to two ASCII code characters and writes them at the specified address of V-RAM.
   b) HEX 4AS: Converts a 16-bit binary number (four hexadecimal digits) to four ASCII code characters and writes them at the specified address of V-RAM.
   c) MNEM DP: Displays a mnemonic code (6-bit ASCII code characters).
   d) CPSET: Sets the character pointer at the specified address.
   e) HSM RD: Reads the next data from the high-speed memory (HSM) and judges whether the data has a trigger pattern. It also checks whether the next data exists in the HSM; if not, displays +++ and returns from the personality program to the main program (ROM1).
   f) STR CHK: This is a trigger check routine used by HSM RD.

7.5 PERSONALITY PROGRAM OPERATION

Most of the personality program (ROM2) is used for the disassemble function. Since 8-bit microprocessors usually have variable-length instructions, the HSM must sometimes be accessed more than once to display one line. (See Fig. 7.7 for the basic flowchart of the personality program.)

A disassemble routine is used only for OP codes in the mnemonic mode; absolute mode routines are used in other cases.

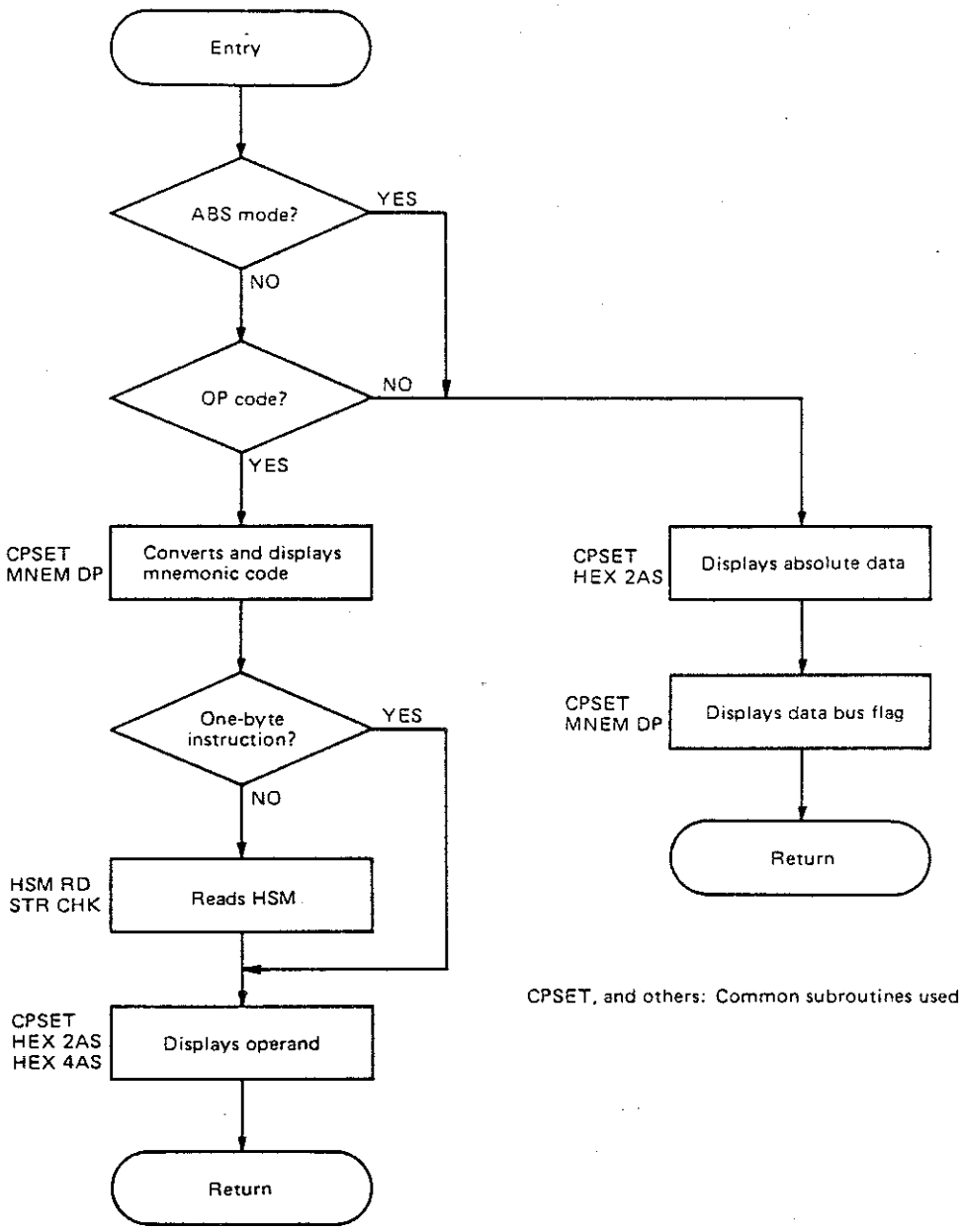


Fig. 7.7 Personality program flowchart

CHAPTER 8
TROUBLESHOOTING

8.1 GENERAL

This chapter explains troubleshooting for the TR4720-540 Z80 Personality Kit using flowcharts. (Refer to the TR4720 Instruction Manual for the basic functions, operations, and principles of operation of the logic analyzer.) After troubleshooting, test the personality kit performance and adjust the CRT display.
The part numbers and symbols used in this chapter are the same as those printed or marked in the circuit drawings and on boards. (Refer to 7.2 "Signal Names" and Appendix in the TR4720 Instruction Manual.)

8.2 TROUBLESHOOTING PREPARATIONS

Tables 8.1 and 8.2 list the units and tools necessary for troubleshooting; use units listed in Table 8.1 or their equivalents.

Table 8.1 Equipments necessary for troubleshooting

Equipment	Specifications	Recommended equipment
Logic analyzer	State and timing display Measurement object microprocessor: Z 80 Clock frequency: 10 MHz	TR4720 TR4720-540 Manufactured by ADVANTEST
Digital multimeter	DC voltage measurement range: 0 to ±1000 V DC voltage measurement accuracy: ±0.1% of rdg. or more AC voltage measurement range: 0 to 1000 V Resistance measurement range: 200 Ω to 1 MΩ Resistance measurement resolution: 10 mΩ or more	TR6855 Manufactured by ADVANTEST
Oscilloscope	Frequency range: 10 MHz or more Input sensitivity: 10 mV/DIV or more	
Printer	Interface: Current loop	EPSON MP-80 Manufactured by Shinshu Seiki Co., Ltd.

Table 8.2 Tools necessary for troubleshooting

Toll	Stock number	Remarks
Connection cable	HIF3-40D-AC (30)	Manufactured by Hirose Electric Co., Ltd.
Connection cable	DCB-RR0771-1 DCB-RR0010A-1	
Adjustment board	AAA-CZ583-1	50 pins (double)

Set of troubleshooting tools: Phillips screwdrivers (2.6 mm and 3.0 mm), standard screwdriver (2 mm), soldering iron (30 W), tweezers, pliers, and wire cutter.

8.3 PERSONALITY BOARD MOUNTING AND DEMOUNTING

1) Set the POWER switch to OFF.
2) Remove four Phillips screws (3 mm) fixing the main unit upper cover, then remove the upper cover.
3) The personality board is at the right end as viewed from the front panel. Remove three connectors on top of the personality board, then pull out the personality board.
4) Uncover the personality board and mount it via the adjustment board. When observing the test output signal, use the cable connector HIF3-40D-AC(30) in place of the flat cable FCA-0007. Also, when connecting the CPU PROBE and the personality board, use DCB-PR0010A-1 in place of FCA-0011.

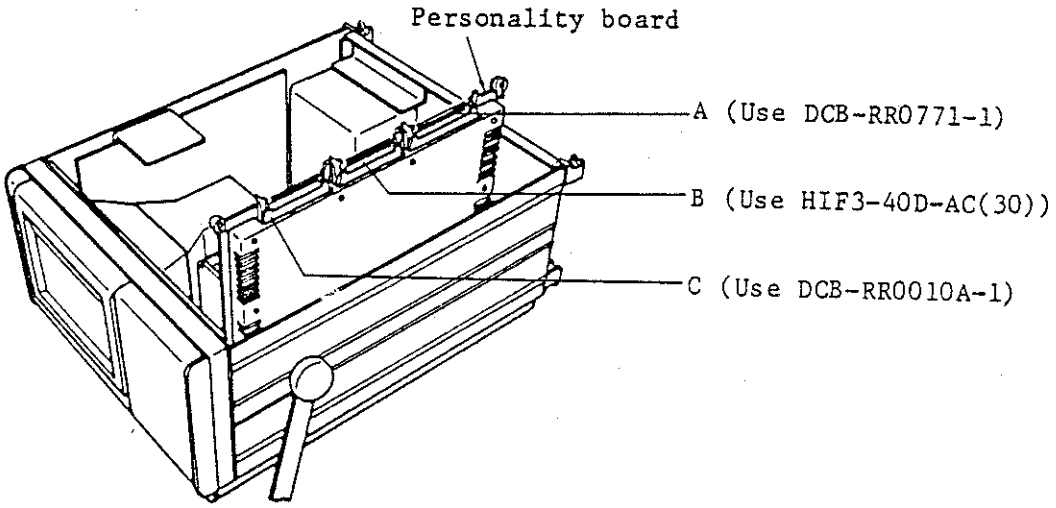


Fig. 8.1 Personality board mounting and demounting

8.4 GENERAL PRECAUTIONS

1) Chapter 8 has been prepared especially for electronic engineers and those who have experience in repairing measurement units; they must understand the entire contents.
2) Use power of 100 (120, 200, 220, or 240) VAC ±10%, 50 or 60 Hz.
3) The power cable plug has three prongs; the round prong in the center is for ground. If this plug is connected to an AC receptacle via an 2-prong adapter, be sure to ground the wire led out from the adapter, or ground terminal GND on the rear panel.
4) Perform troubleshooting in a location free from dust, vibration, noise, and so forth.
5) Set the POWER switch to OFF before checking inside the unit and mounting/demounting the personality board.
6) When an oscilloscope, digital voltmeter, or logic analyzer is used, take care not to toutch to unneccessary terminals or lead wires.
7) Use a 20 W or 30 W soldering iron to change faulty parts on the personality board and perform soldering without undue delay. If a soldering iron is used on the personality board overly long, parts (especially, semiconductors) or print patterns may be damaged. It is advisable to use a solder absorber when removing parts having many pins, such as integrated circuits.
8) When changing parts, use parts listed in the parts list in the back of this manual or their equivalents. Contact the ADVANTEST's head office or your nearest agent for parts marked with asterisks in the parts list.
9) Be careful of electric shock; this is a high voltage unit. Wait 5 minutes or more after cutting the power off to change parts.
10) To prevent damage to CMOS ICs by static electricity, observe the following:
    - Minimize handling of CMOS ICs.
    - Store CMOS ICs in a conductive case to prevent build up of static electricity.

- Discharge static electricity from your body by touching a grounded conductive object before handling CMOS ICs and do not wear clothing made of synthetic fibers.
- Do not touch CMOS IC pins directly with hands.
- Carry CMOS ICs in a anti-static container.
- Do not slide CMOS ICs over any surface.
- Keep synthetic products such as plastics and vinyls away from the work table.
- Ground the work tables and chairs.
- Use a soldering iron with little leakage current peculiar to CMOS ICs and ground the iron tip via a resistor of approximately 100 kΩ (for slow leakage).

11) Before troubleshooting, refer to 3.5 "Operation Check" in the TR4720 Instructions Manual to check that the related troubles are not caused by operation errors.

12) If the same trouble occurs when other personality kits are used, the unit itself may be faulty; in this case, refer to Chapter 6 "Troubleshooting" in the TR4720 Instructions Manual.

8.5 PERSONALITY KIT TROUBLESHOOTING

① Connect the microprocessor probe to the CPU PROBE connector on the lower part of the TR4720 front panel.

② Connect the other end of the microprocessor probe to the CPU PROBE TEST receptacle on the TR4720 rear panel.
If a 40-pin DIP plug connector is used, connect it directly to the CPU PROBE TEST receptacle; if a 40-pin DIP clip connector is used, connect it via the attached 40-pin DIP IC package. (See Fig. 8.2.)

③ Press the TRACE key to set the TRACE STATE ALL measurement mode.

④ Press the DEFAULT key to initialize all trace conditions.

⑤ The input prompt is placed at the TRIG- ADRS position; input 0000 with the ENTRY key.

⑥ Press the RUN key in the EXECUTE section. The test pattern is displayed on the CRT display. (See Fig. 6.10)

⑦ If the test pattern shown in Photo Fig. 6.6 is not displayed, the microprocessor probe or the personality board may be faulty. Check the microprocessor probe for broken cable or loose connector contacts.

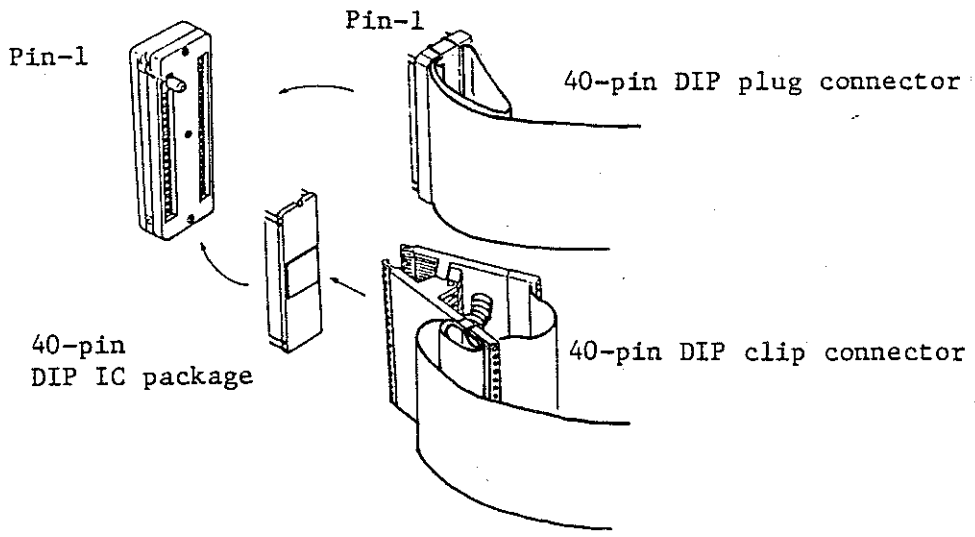


Fig. 8.2 Connection to CPU PROBE TEST receptacle

CHART 1 Microprocessor Probe and Connector Check

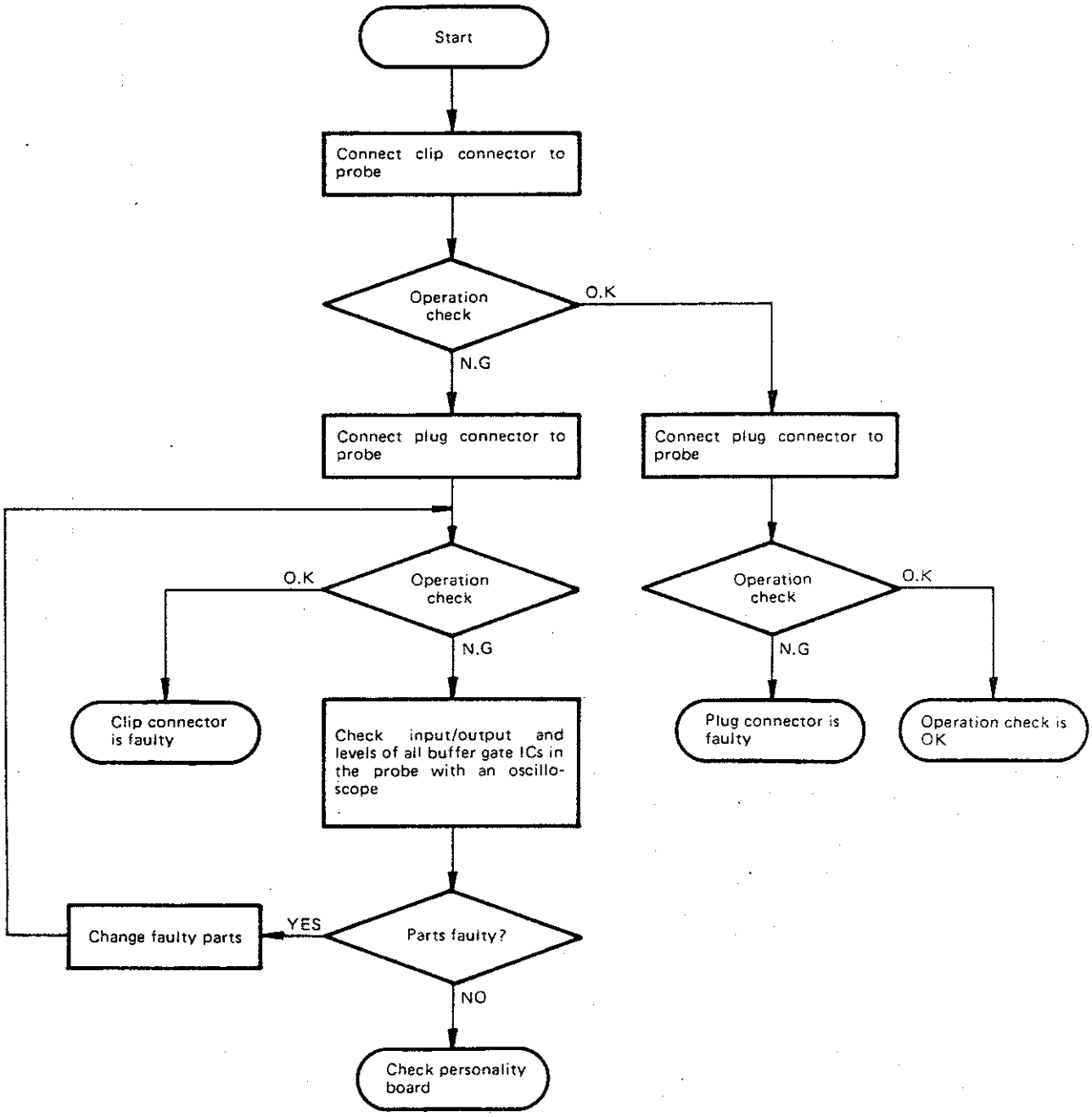


CHART 2 SUT Connection Check

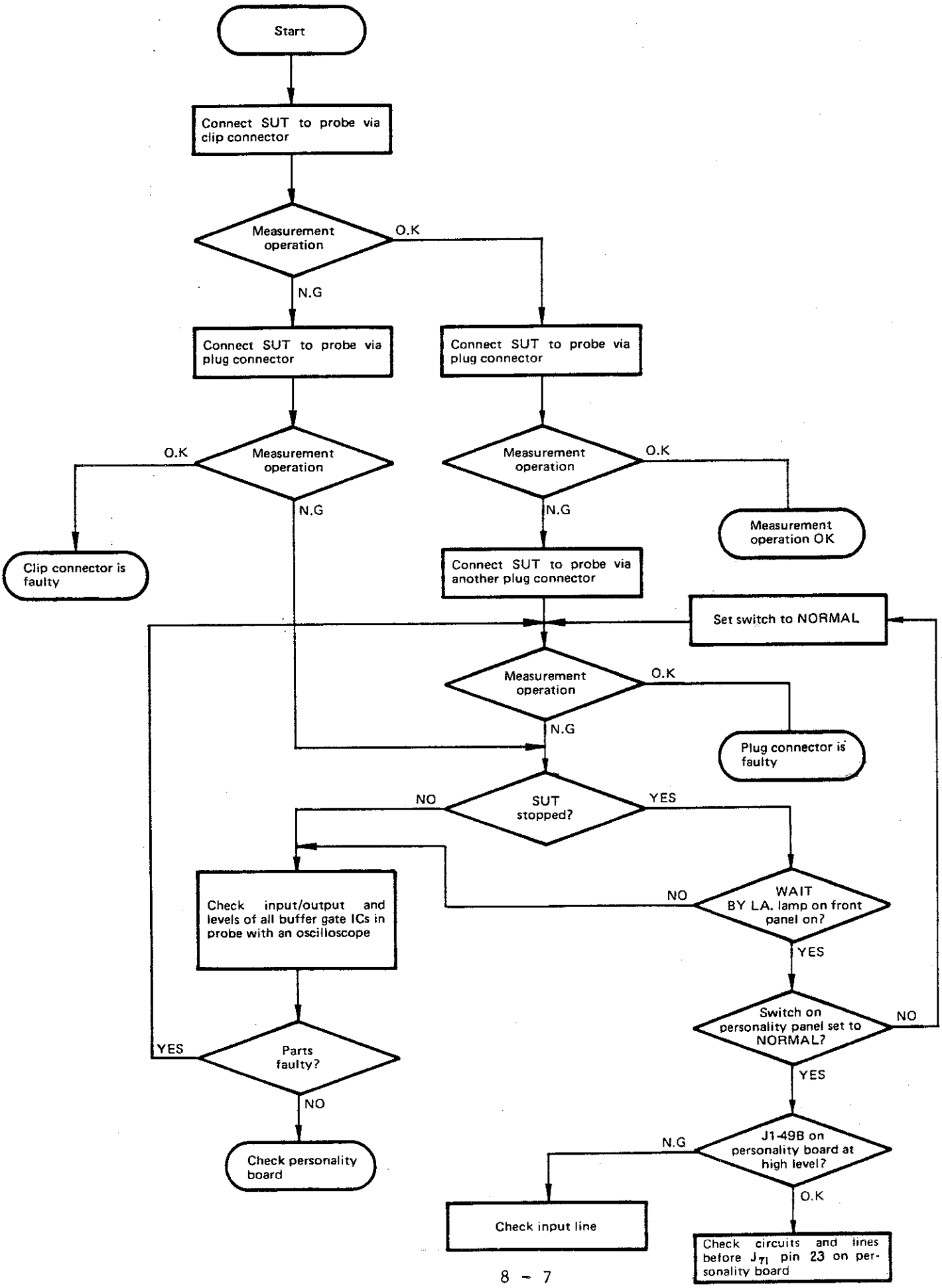
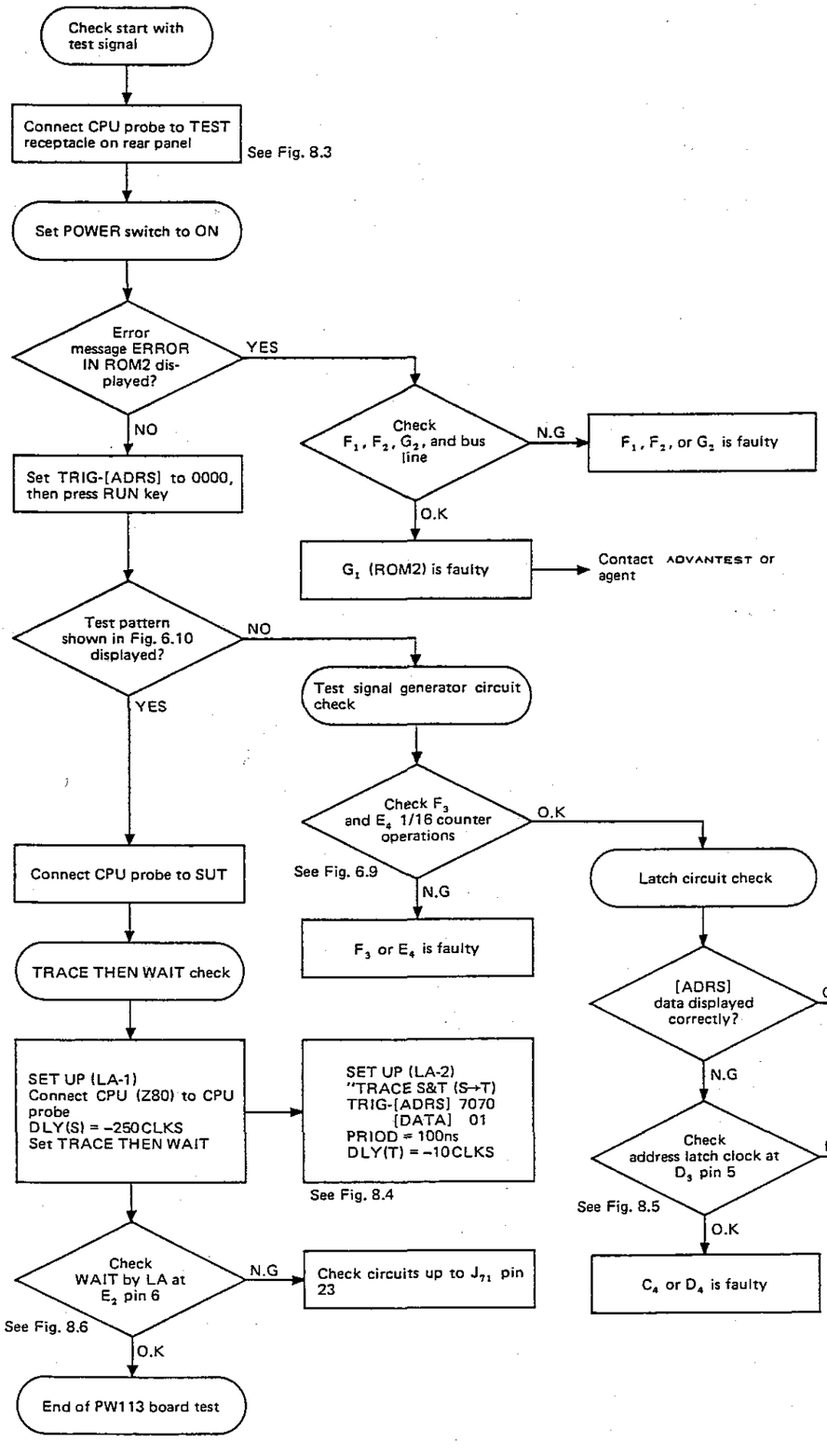


CHART 3 Personality Board (PW113) Check



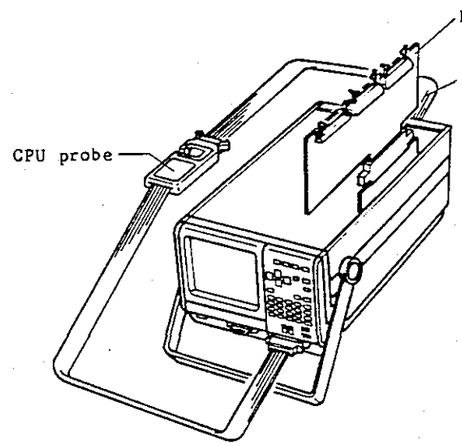


Fig. 8.3 Setup (1)

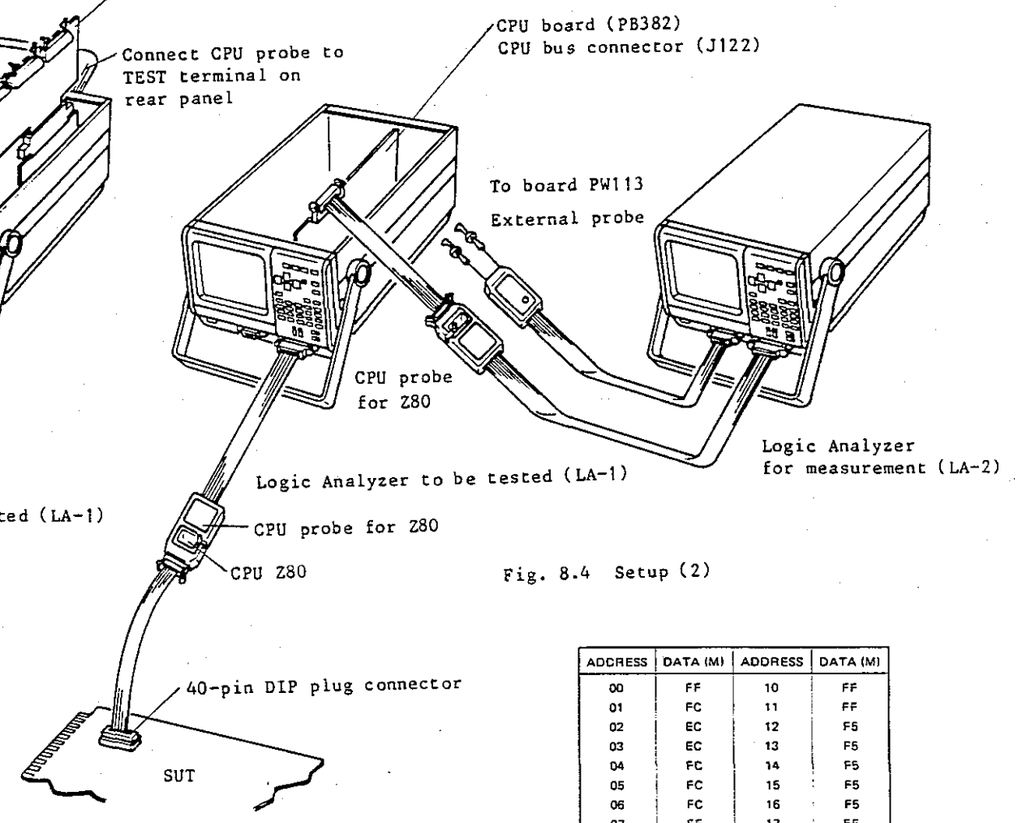


Fig. 8.4 Setup (2)

ADDRESS	DATA (M)	ADDRESS	DATA (M)
00	FF	10	FF
01	FC	11	FF
02	EC	12	F5
03	EC	13	F5
04	FC	14	F5
05	FC	15	F5
06	FC	16	F5
07	FF	17	FF
08	FF	18	FF
09	FE	19	FF
0A	EE	1A	F3
0B	EA	1B	F3
0C	FA	1C	F3
0D	FA	1D	F3
0E	FA	1E	F3
0F	FF	1F	FF

Table 8.1 Test signal ROM (F_4) programs

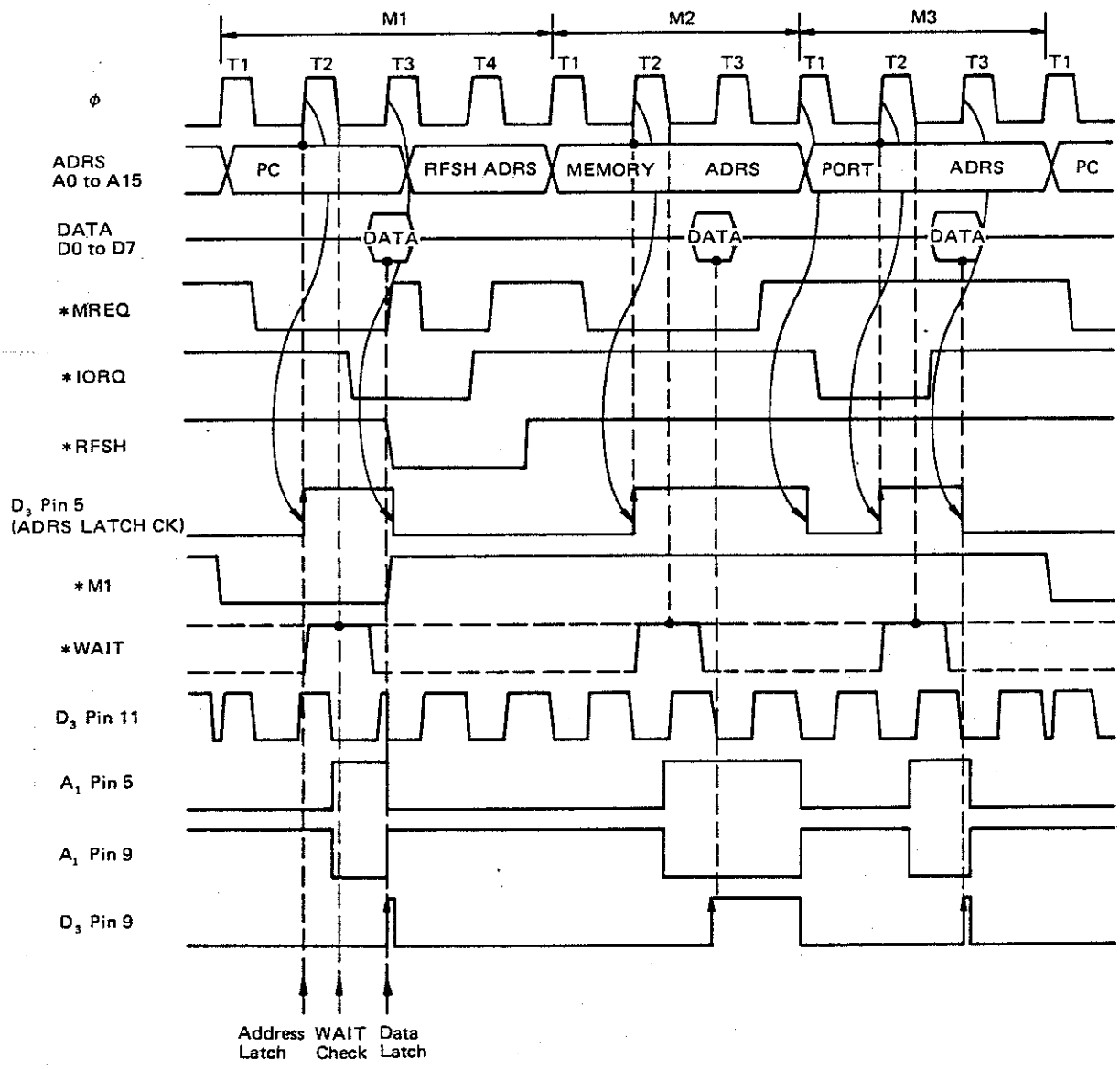
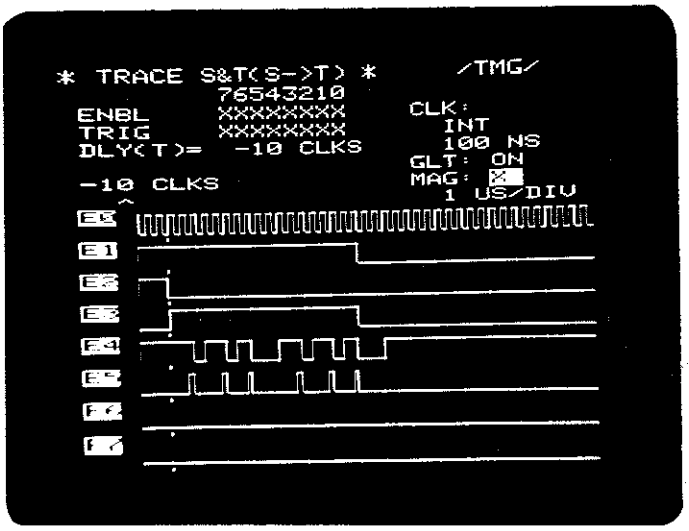


Fig. 8.5 Timing chart of sampling (latch)



E_0: B_5 Pin 4 (ϕ)
E_1: E_2 Pin10 (*DLY OVER FLOW)
E_2: D_1 Pin 5 (CTR INH)
E_3: E_2 Pin 6 (*WAIT BY LA)
E_4: D_4 Pin11 (ADDR Latch CK)
E_5: A_4 Pin11 (DATA Latch CK)
E_6: D_1 Pin 1 (NOT TRACE)
E_7: D_1 Pin 3 (*TRACE then WAIT)

Fig. 8.6 Timing of WAIT by LA [DLY(S)=-250CLKS]

CHAPTER 9
PARTS LIST, PARTS LOCATIONS AND CIRCUIT DIAGRAMS

9.1 GENERAL

This chapter lists the electrical and mechanical parts used in the TR4720 Logic Analyzer Parsonality Kits. When replacing a defective electrical part, confirm its specification by referring to the parts description and use the same or equivalent part.
When ordering parts from us, indicate part and stock numbers for electrical parts or part names and stock numbers for mechanical parts.

NOTES

The parts and specifications are subject to change without prior notice to meet the users' requiremeents or improve the ADVANTEST's quality control.

9.2 SYMBOLS AND ABBREVIATIONS

The symbols and abbreviations used in this chapter are indicated in Table 7.1 in the Instruction Manual of the TR4720 Logic Analyzer. Signal names are included in Table 7.2 in the main Instruction Manual. As for the abbreviations of the annotations on the display, see Appendix 1.

Fig. & Index No.	Stock No.	Description	
9-1	MMX-14941A-1	COVER, top	
	MMX-14940A-1	COVER, bottom	
9-2	MBT-14710B-1	COVER, top	
	MBT-14709A-1	COVER, bottom	
	MKN-10434A-1	SPACER	

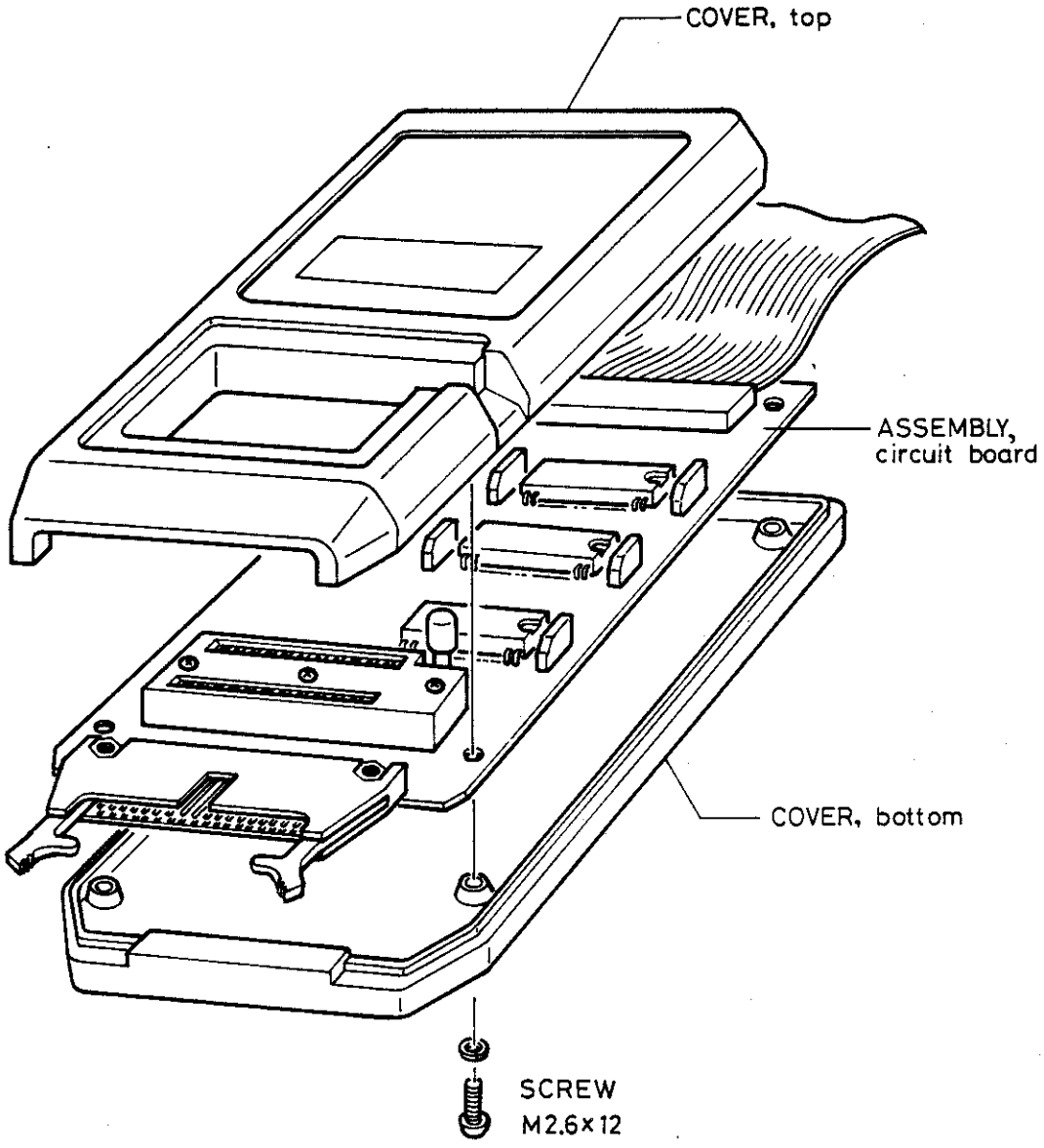


Fig. 9-1
MICROPROCESSOR PROBE
MECHANICAL PARTS

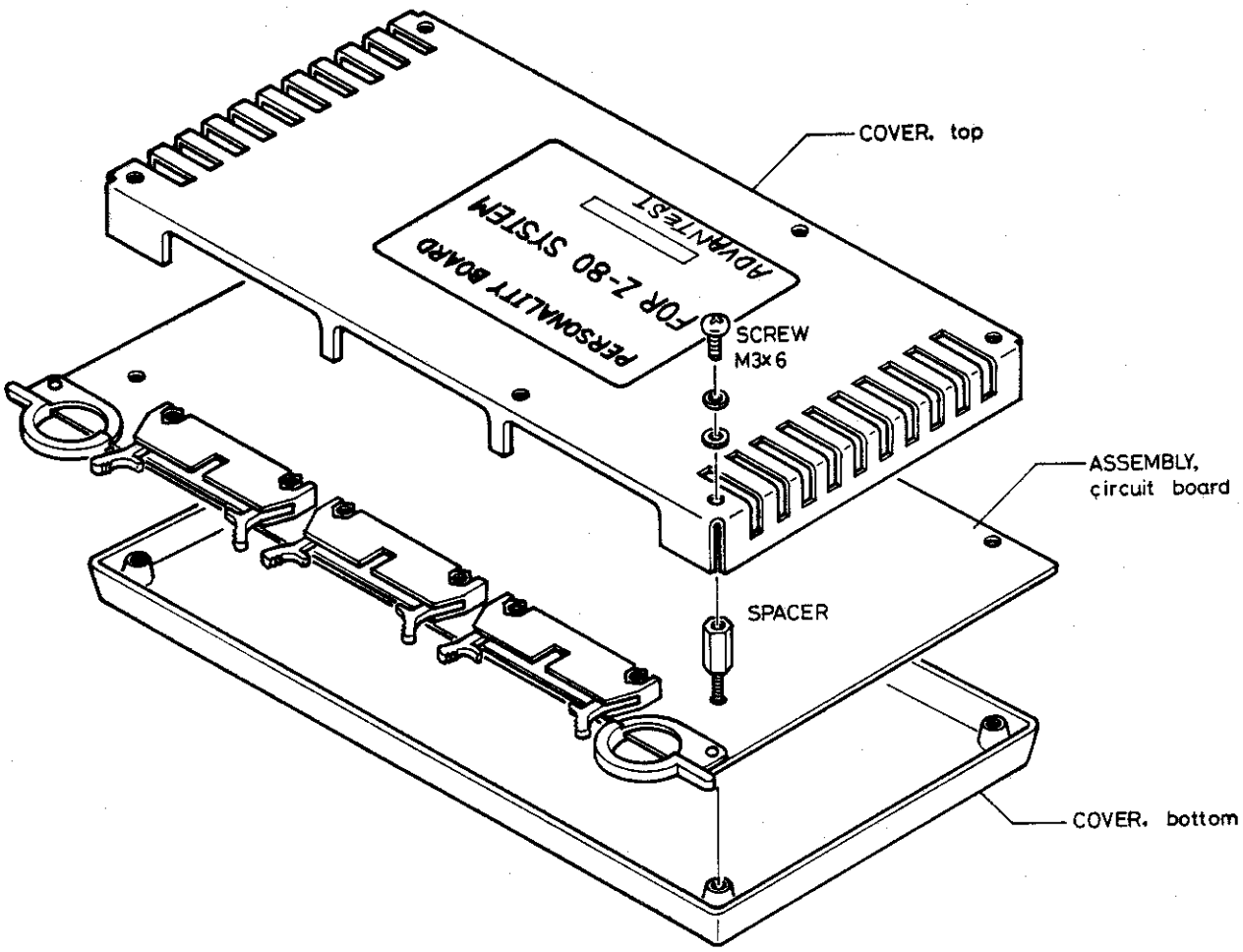


Fig. 9-2
PERSONALITY BOARD
MECHANICAL PARTS

TR4720-540
Z80 CPU PROBE
SV204

Parts No.	Stock No.	Description	
SV204 - IC1	SN74LS244N	IC: Octal Buffer/Line Driver/ Line Receiver Low Power	
" - IC2	SN74LS244N	IC: Octal Buffer/Line Driver/ Line Receiver Low Power	
" - IC3	SN74LS00N	IC: Quadruple 2-Input NAND Gate Low Power	
" - IC4 thru " - IC6	SN74LS244N	IC: Octal Buffer/Line Driver/ Line Receiver Low Power	
" - C21 thru " - C26	244M1602-335M	C: FXD ELECT TANTAL 3.3μF ±20% 16V	
" - J33	240-3346	IC Socket	
" - J34	HIF3-409-2.54DS	Connector	
" - J35	MC-66A	Cable	
" - R41 thru " - R48	RD12S 820ΩJ	R: FXD CAR 820Ω ±5% 1/8W	
" - R49 thru SV204 - R56	RD12S 12KΩJ	R: FXD CAR 12KΩ ±5% 1/8W	
	MI-66B	Cable	
	MI-67A	Cable	

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PW113

Parts No.	Stock No.	Description	
PW113 - IC1A	SN74LS74AN	IC: Dual D-Type Edge-Triggered Flip Flop Low Power	
" - IC2A	SIS-000038	IC: Written	
" - IC3A	SN74LS30N	IC: 8-Input NAND Gate Low Power	
" - IC4A	SN74LS374N	IC: Octal D-Type Flip-Flop Low Power	
" - IC5A	SN74LS241N	IC: Octal Buffer/Line Driver/ Line Receiver Low Power	
" - IC1B	SN74LS02N	IC: Quadruple 2-Input NOR Gate Low Power	
" - IC2B	SN74LS374N	IC: Octal D-Type Flip-Flop Low Power	
" - IC3B	SN74LS04N	IC: Hex Inverter Low Power	
" - IC4B	SN74LS00N	IC: Quadruple 2-Input NAND Gate Low Power	
" - IC5B	SN74LS241N	IC: Octal D-Type Flip-Flop Low Power	
" - IC1C	SN74S51N	IC: Dual 2-Wide 2-Input AND -OR- Invent Gate	
" - IC2C	SN74LS74AN	IC: Dual D-Type Edge-Triggered Flip-Flop Low Power	
" - IC4C	SN74LS374N	IC: Octal D-Type Flip-Flop Low Power	
" - IC5C	SN74LS241N	IC: Octal D-Type Flip-Flop Low Power	
" - IC1D	SN74LS04N	IC: Hex Inverter Low Power	
" - IC2D	SN74LS00N	IC: Quadruple 2-Input NAND Gate Low Power	
" - IC3D	SN74S74N	IC: Dual D-Type Edge-Triggered Flip-Flop	
" - IC4D	SN74LS374N	IC: Octal D-Type Flip-Flop Low Power	
" - IC5D	SN74LS241N	IC: Octal D-Type Flip-Flop Low Power	
" - IC2E	SN74LS20N	IC: Dual 4-Input NAND Gate Low Power	
PW113 - IC4E	SN74LS161AN	IC: Synchronous 4-Bit Counter Low Power	

Parts No.	Stock No.	Description	
PW113 - IC5E	SN74LS241N	IC: Octal D-Type Flip-Flop Low Power	
" - IC1F	SN74LS244N	IC: Octal Buffer/Line Driver/ Line Receiver Low Power	
" - IC2F	SN74LS04N	IC: Hex Inverter Low Power	
" - IC3F	SN74LS161AN	IC: Synchronous 4-Bit Counter Low Power	
" - IC4F	SIS-000039	IC: Written PROM (IM5610CPE)	
" - IC5F	SN74LS241N	IC: Octal D-Type Flip-Flop Low Power	
" - IC1G	SIS-000037	IC: Written EP ROM (MB8516)	
" - IC2G	SN74LS30N	IC: 8-Input NAND Gate Low Power	
" - IC3G	SN74LS04N	IC: Hex Inverter Low Power	
" - R36	RD25S 220ΩJ	R: FXD CAR 220Ω ±5% 1/4W	
" - R37	RD25S 1KΩJ	R: FXD CAR 1KΩ ±5% 1/4W	
" - C41	244M1602-335M	C: FXD ELECT TANTAL 3.3μF ±20% 16V	
" - C42	244M51602-335M	C: FXD ELECT TANTAL 3.3μF ±20% 16V	
" - C43		Not assigned	
" - C44	244M1602-335M	C: FXD ELECT TANTAL 3.3μF ±20% 16V	
" - C45	244M1602-335M	C: FXD ELECT TANTAL 3.3μF ±20% 16V	
" - C46		Not assigned	
" - C47	244M1602-335M	C: FXD ELECT TANTAL 3.3μF ±20% 16V	
" - C48	244M1602-335M	C: FXD ELECT TANTAL 3.3μF ±20% 16V	
" - C49		Not assigned	
" - C50	244M1602-335M	C: FXD ELECT TANTAL 3.3μF ±20% 16V	
" - C51	244M1602-335M	C: FXD ELECT TANTAL 3.3μF ±20% 16V	
" - C52		Not assigned	
PW113 - C53	244M1602-335M	C: FXD ELECT TANTAL 3.3μF ±20% 16V	

Parts No.	Stock No.	Description	
PW113 - C54	244M1602-335M	C: FXD ELECT TANTAL 3.3μF ±20% 16V	
" - C55		Not assigned	
" - C56	DM10D 101J3	C: FXD DIPPED MICA 100pF ±5% 300V	
" - J71	609-5007ES	Connector	
" - J72	HIF3-40P-2.54DS	Connector	
PW113 - J73	HIF3-40P-2.54DS	Connector	
	DL2-16A	IC Socket	
	DL2-24A	IC Socket	
	M823(0.8,0.1,6)M003	Bus Bar	

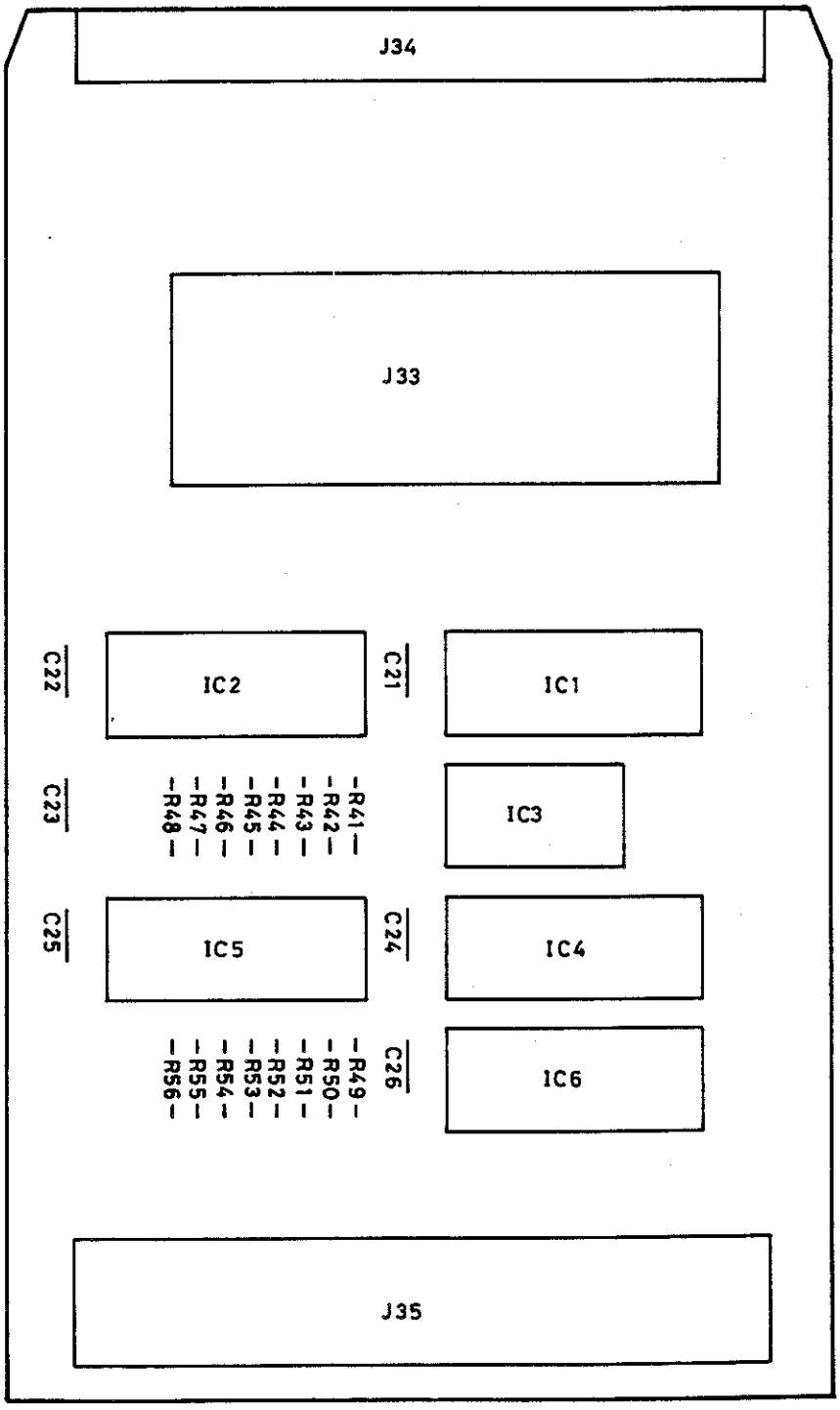


Fig. 9.3 Component locations on SV204

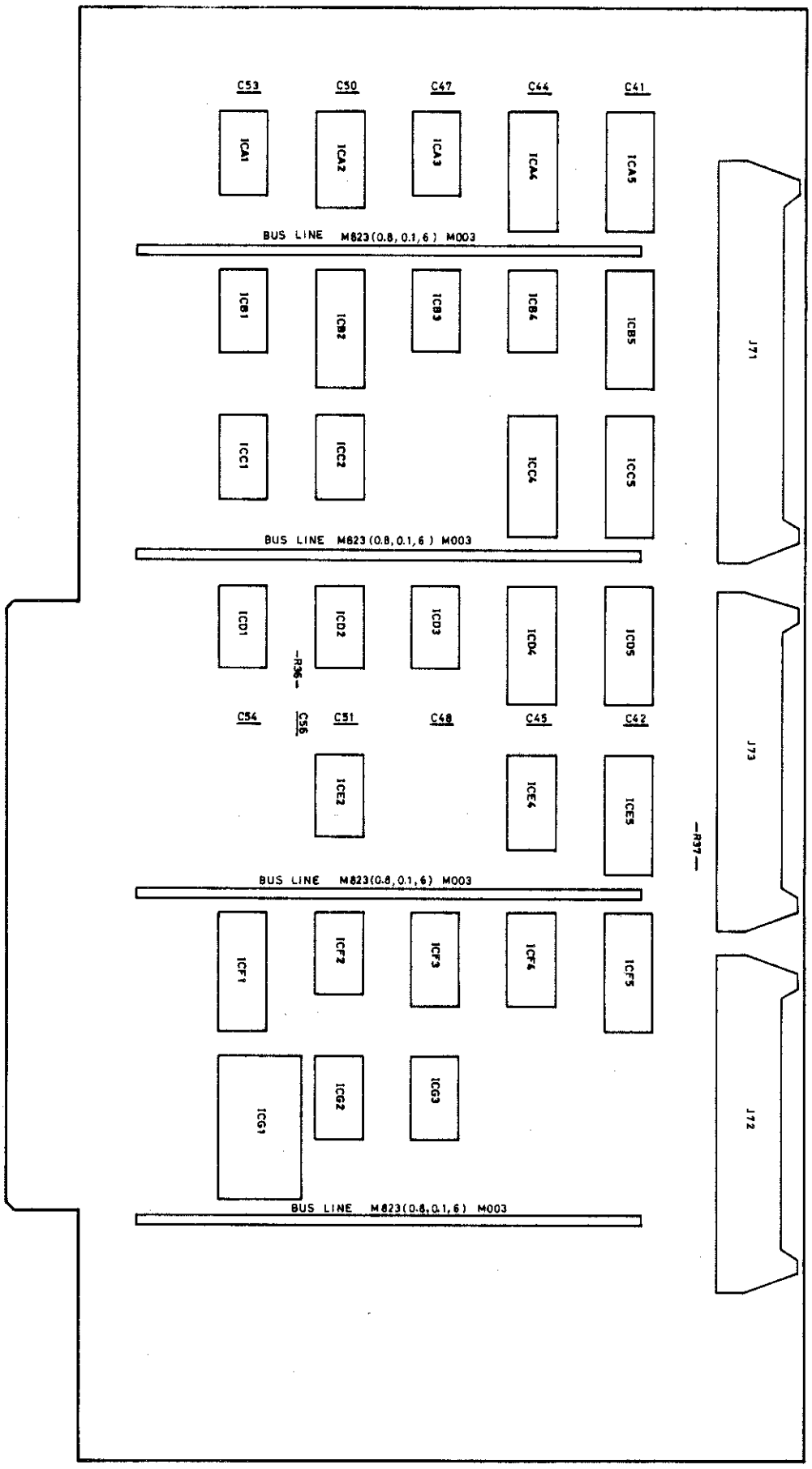
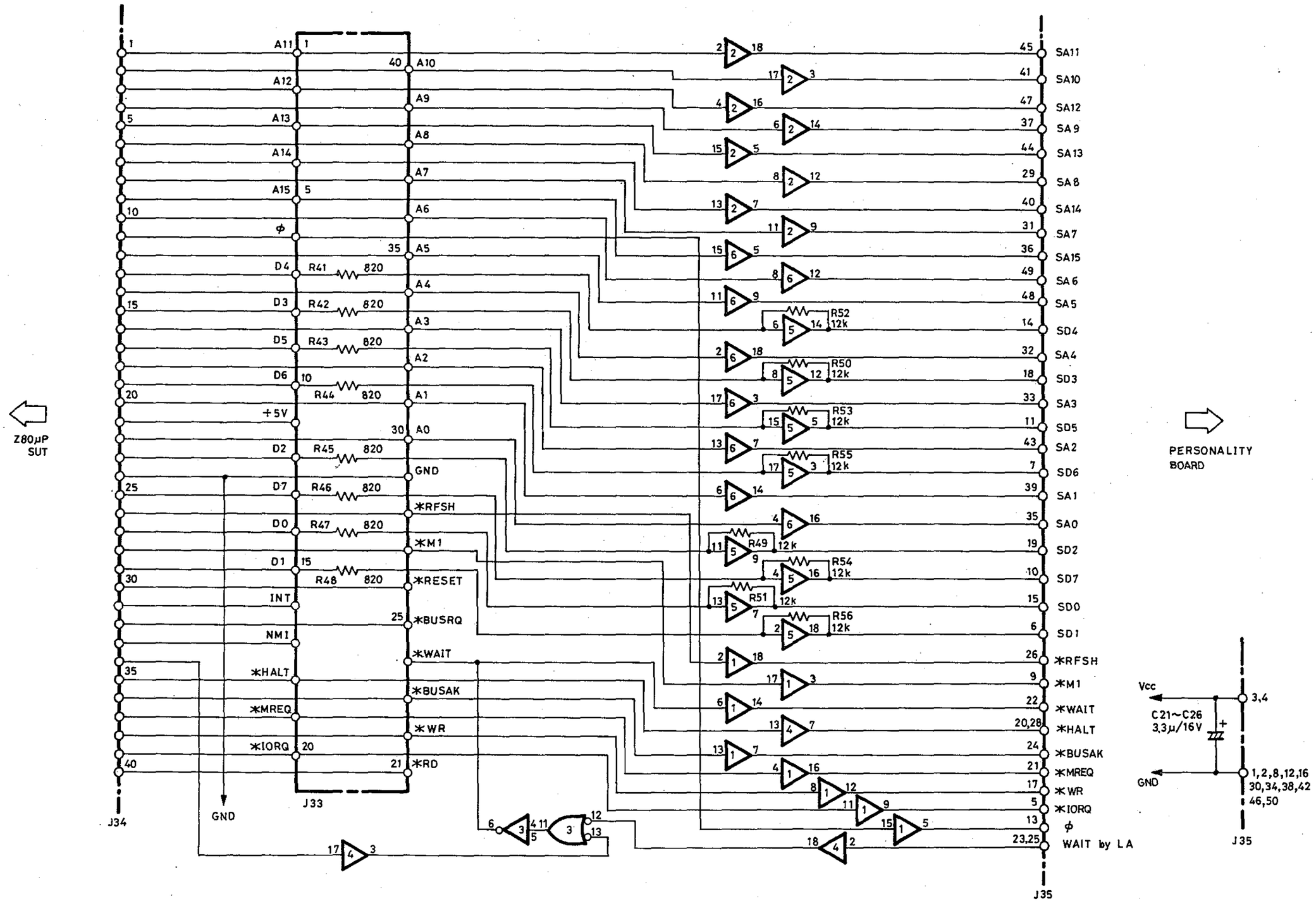


Fig. 9.4 Component locations on PW113



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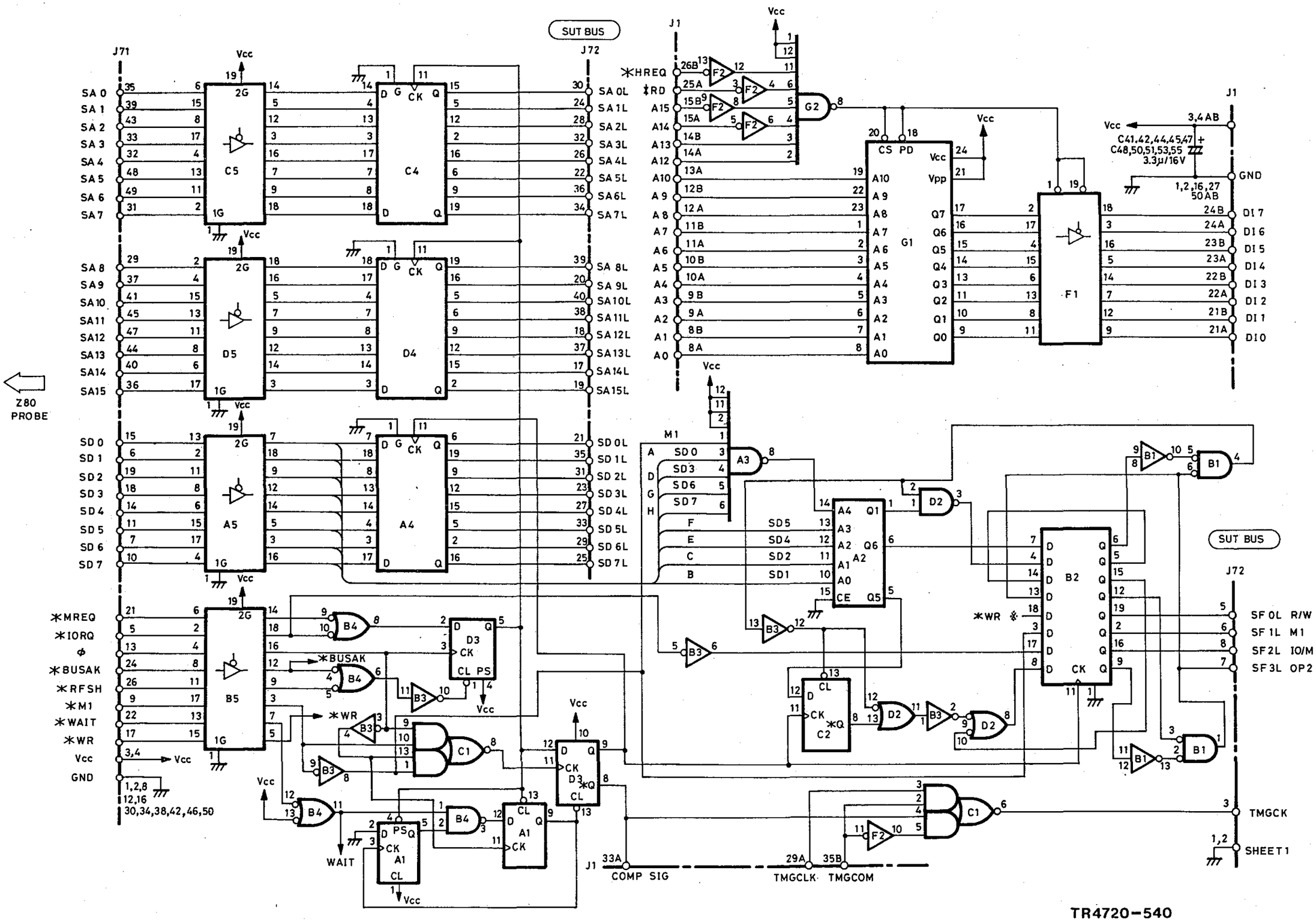
Z80 CPU PROBE
SV204

0820009-001-A



0820009 – 002 – A

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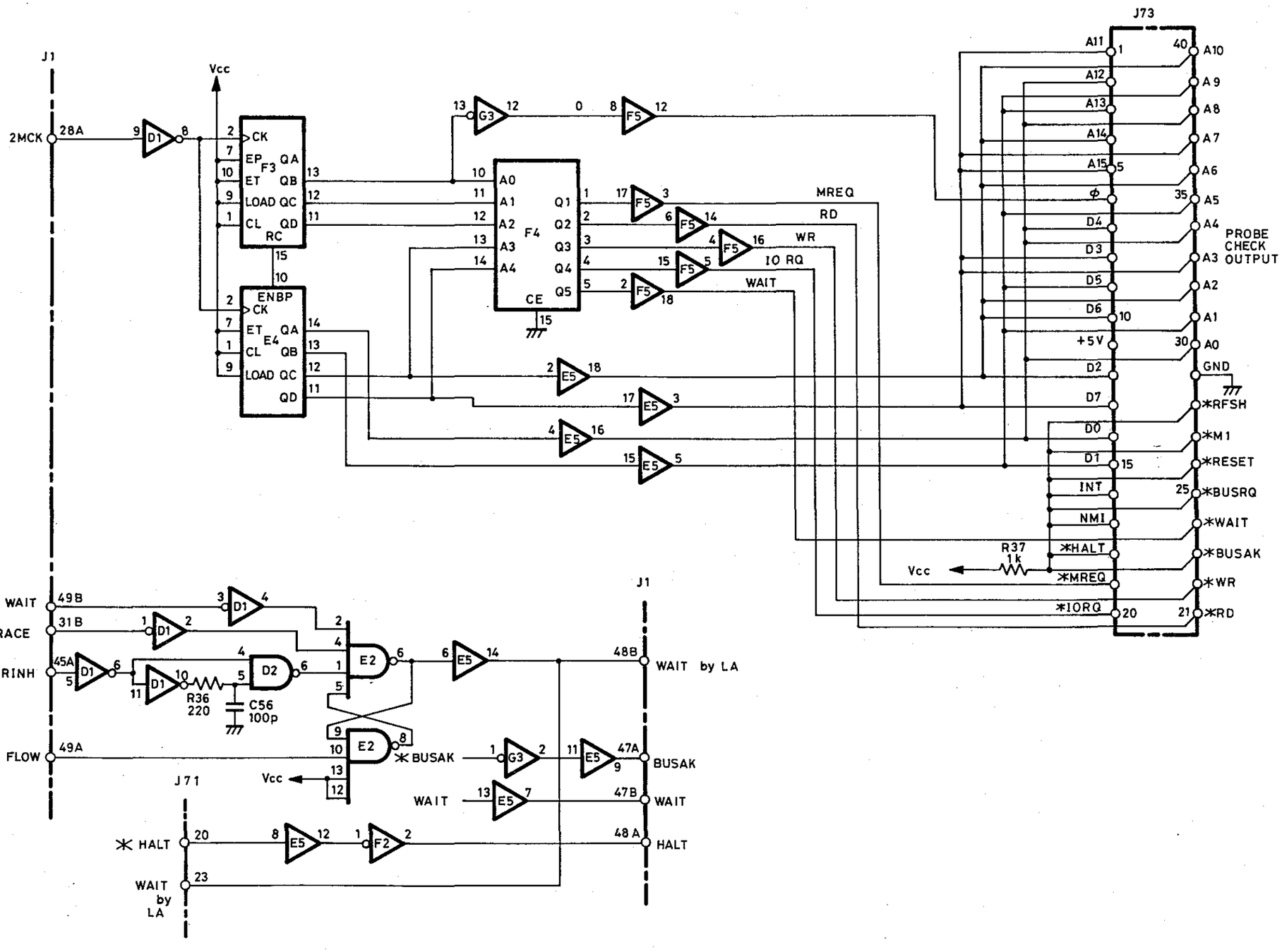
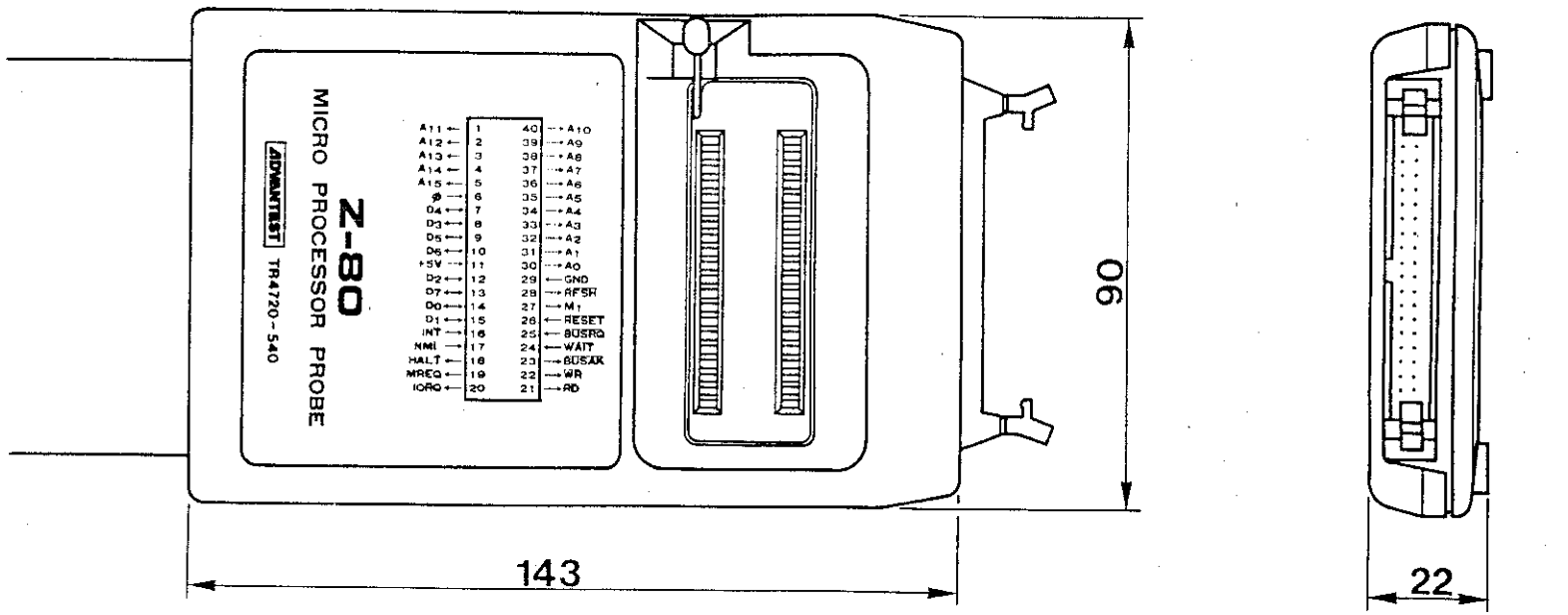
Z80 PERSONALITY BOARD
PW 113 1/2



0820009 – 003 – A

TR4720-540
Z80 PERSONALITY BOARD
PW113 2/2



TR4720-540
EXTERNAL VIEW

4720-540EXT1-606-A

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Advantest's maintenance agreement provides the Purchaser on-site and off-site maintenance, parts, maintenance machinery, regular inspections, and telephone support and will last a maximum of ten years from the date the delivery of the Product. For specific details of the services provided under the maintenance agreement, please contact the nearest Advantest office listed at the end of this Operation Manual or Advantest 's sales representatives.

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